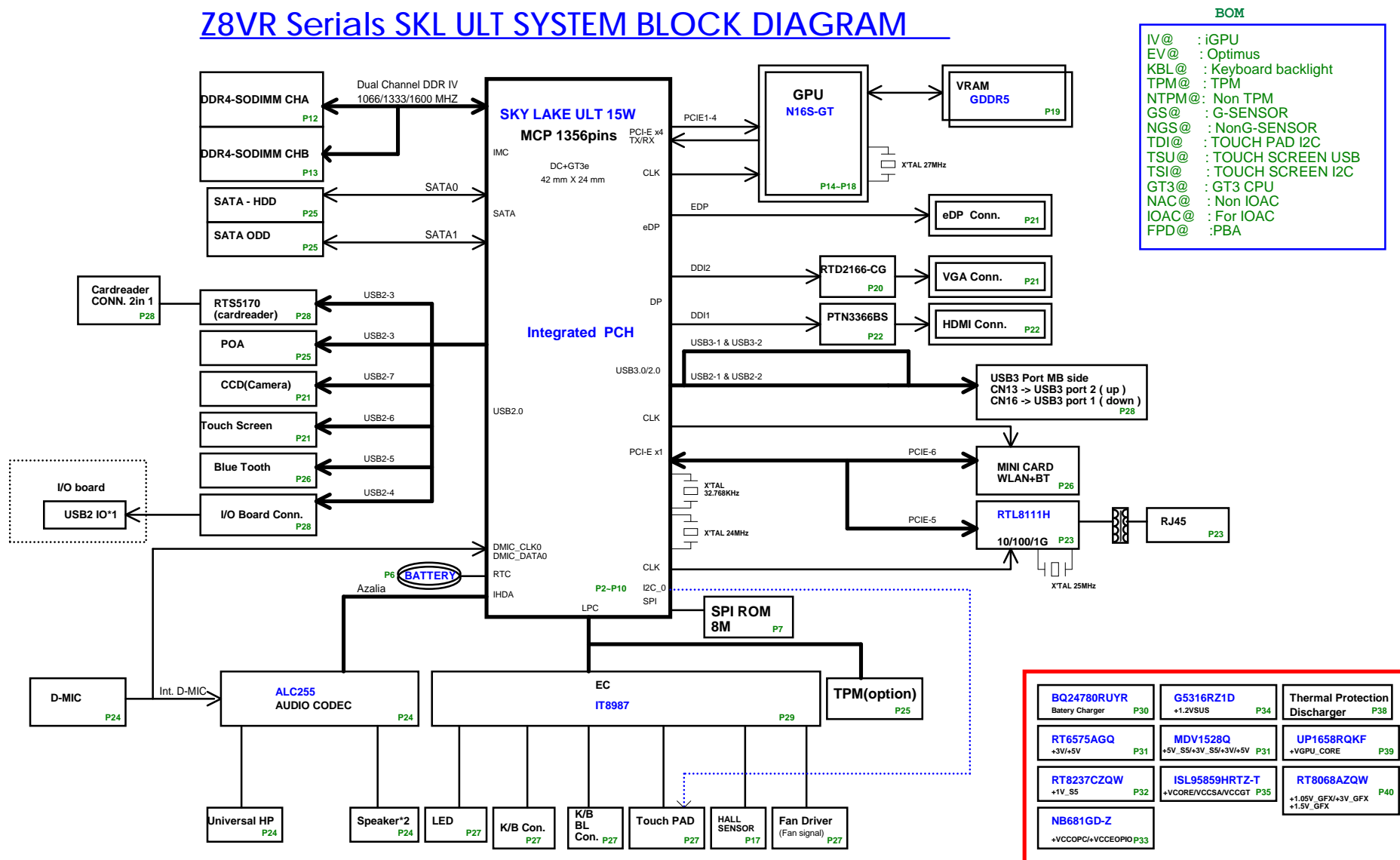
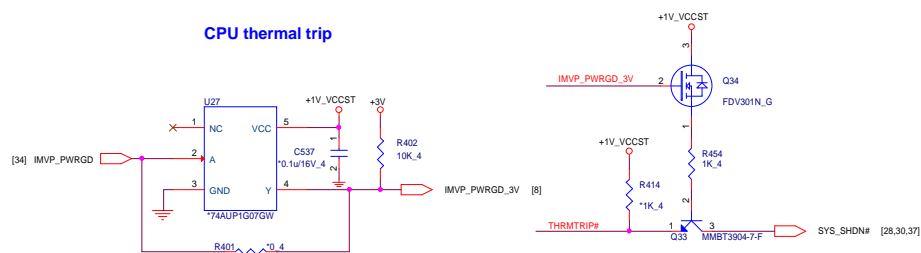
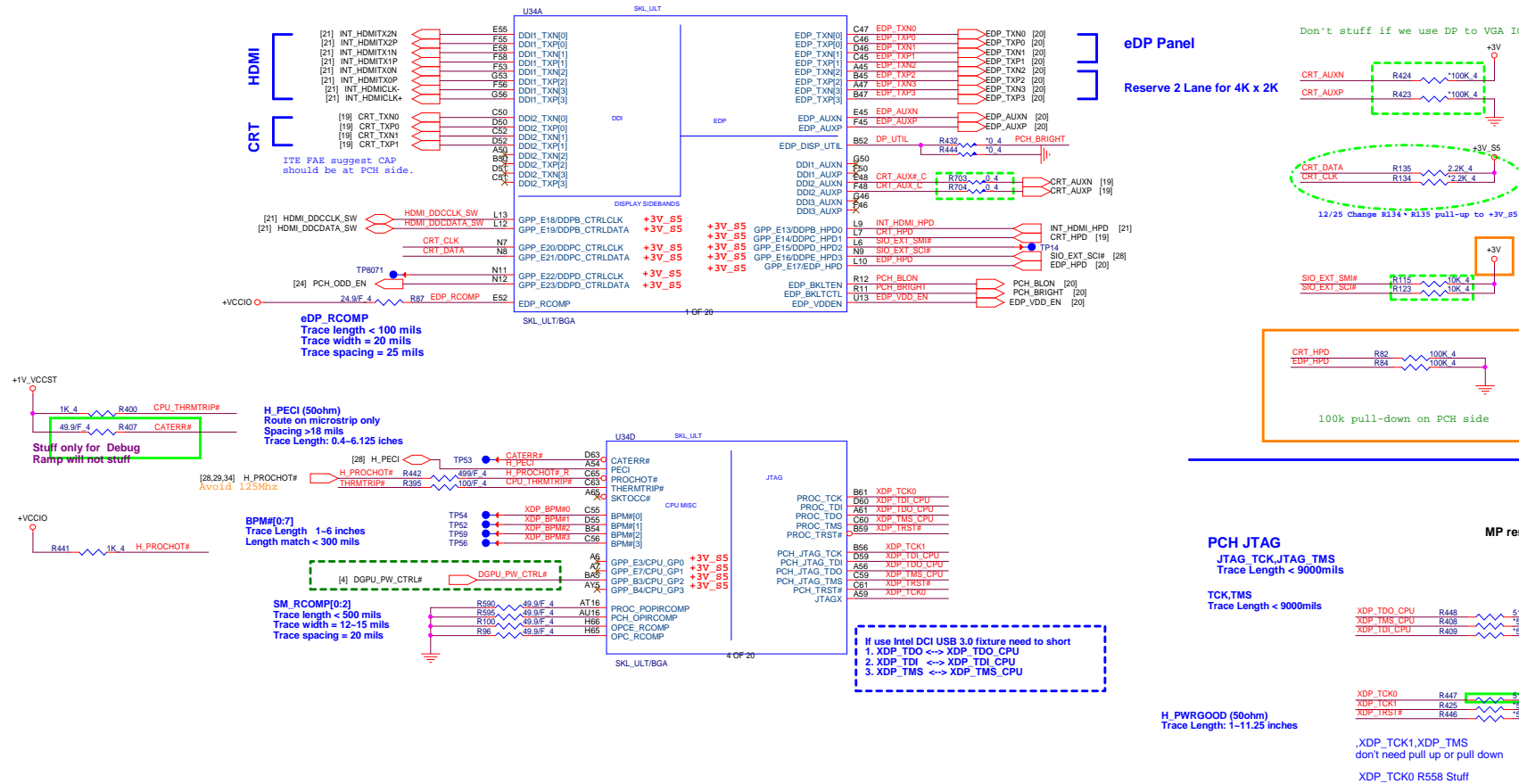


## Z8VR Serials SKL ULT SYSTEM BLOCK DIAGRAM

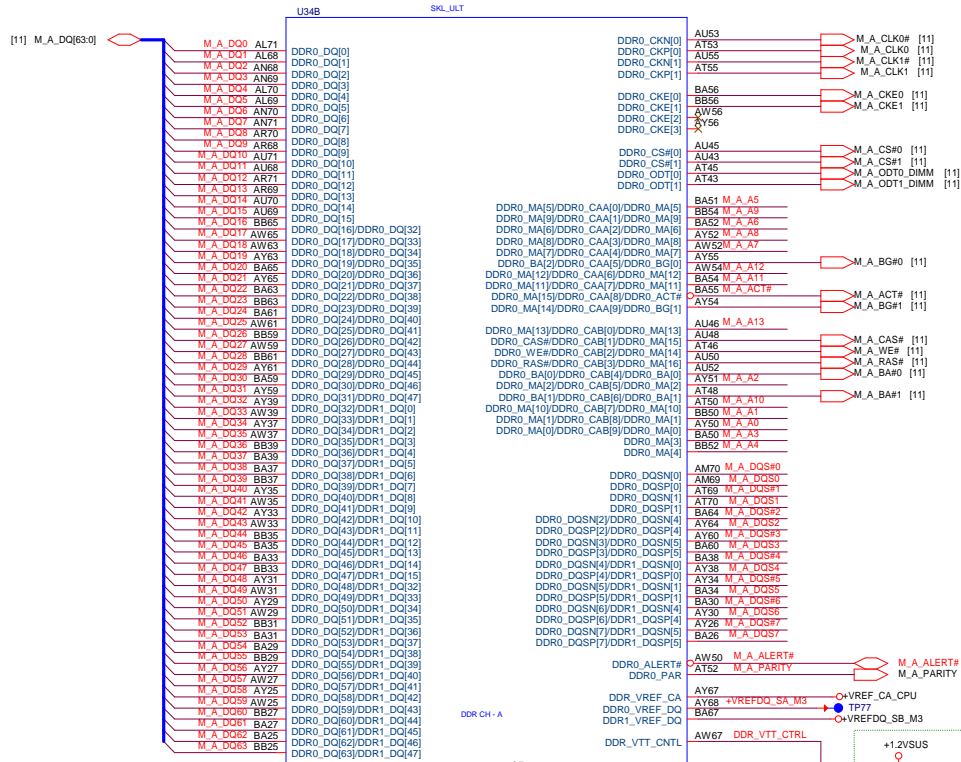


## Skylake ULT (DISPLAY,eDP)

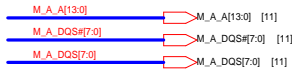
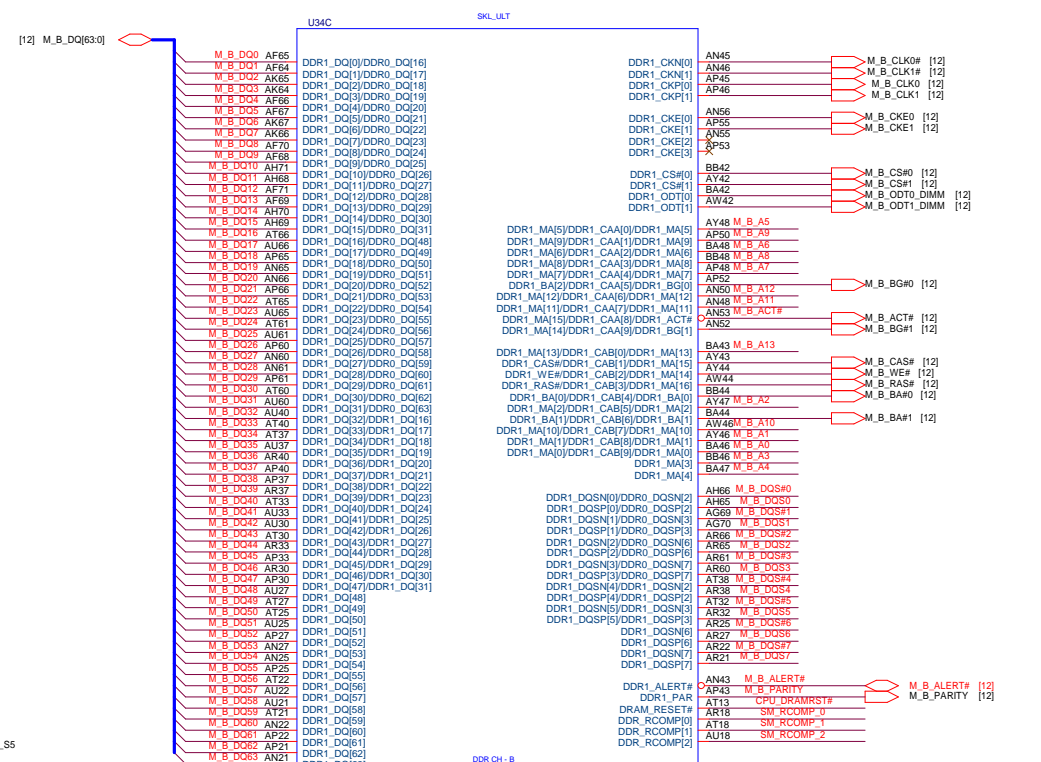


Change Data and DQS to interleave.

## SKL ULT (DDR4)



## SKL ULT (DDR4)

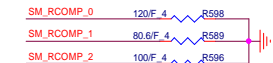
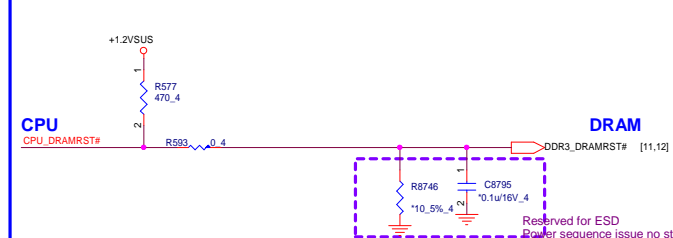


Stuff Q54 for both UMA and GPU in DDR\_VTT\_CNTL



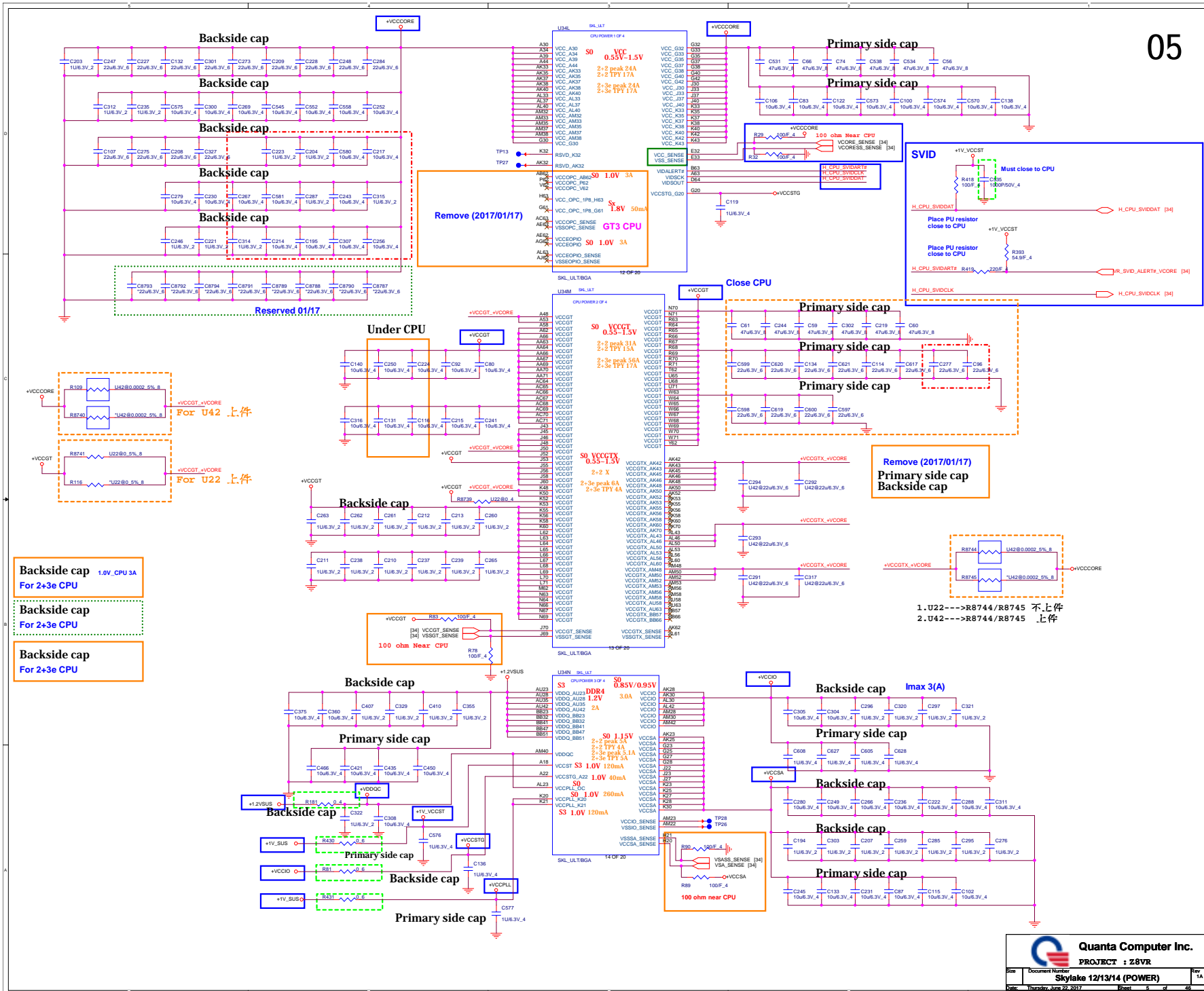
## DRAM COMP

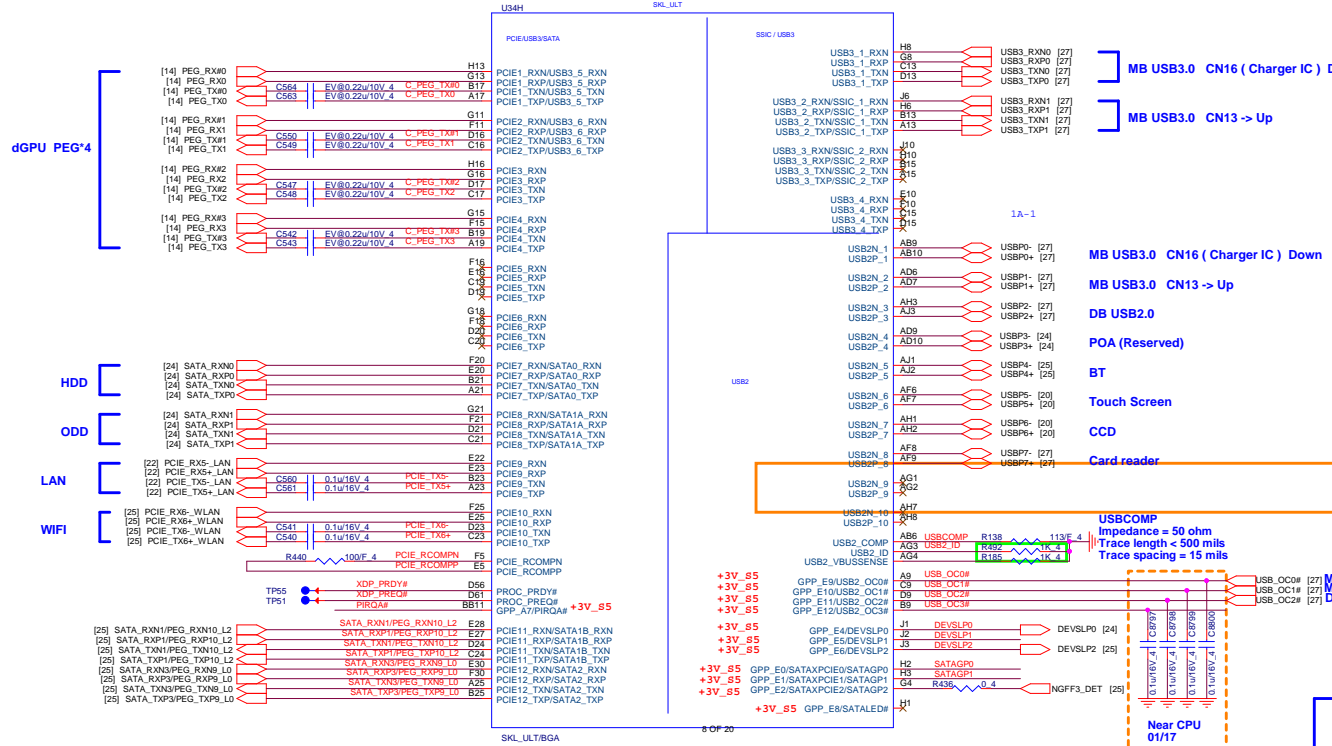
**DRAMRST**

**Quanta Computer Inc.**

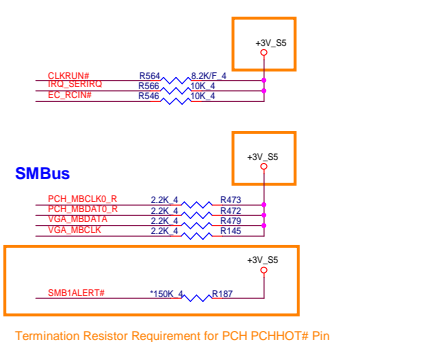
**PROJECT : Z8VR**



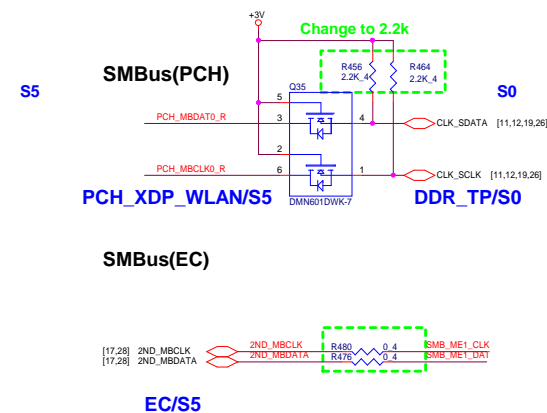




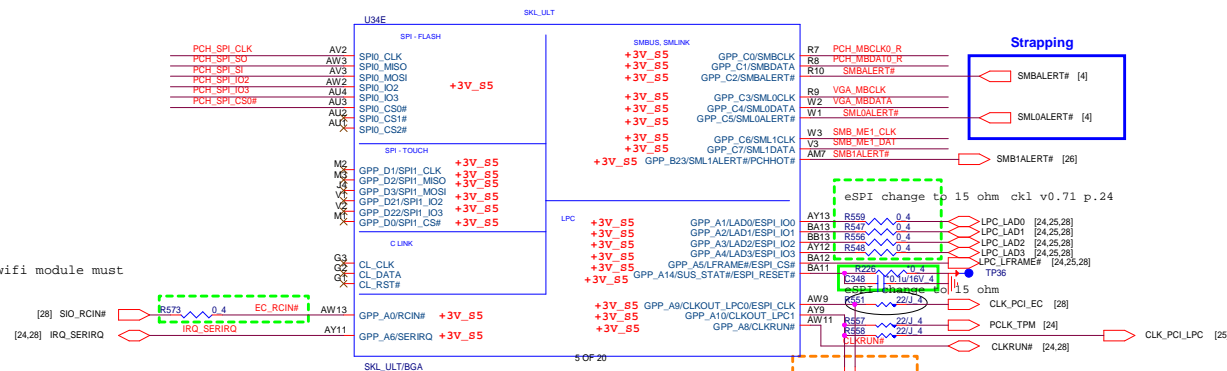




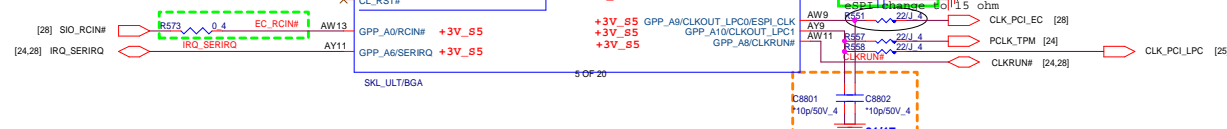
### Termination Resistor Requirement for PCH PCHHOT# Pin Reserve PU 150K resistor



**EC/S5**



For M.2 wifi module must



**PCH SPI ROM(8M)**  
15ohm CS01502JB12  
33ohm CS03302JB29



**SP@ socket P/N: DFHS08FS023 only for A-TEST**

SPI ROM	Vender	Size	Quanta P/N	Vender P/N
Skylake 3.3V	WND	8M	AKE3EFPN07	W25Q64FVSSIQ
	GGD	8M	AKE2EZNOQ00	GD25B64CSIGR
	WND	16M	AKE3DZNO0N1	W25Q128FVSIQ
	GGD	16M	AKE3DZNOQ02	GD25B127DSIGR

3.3K is original and for no support fast read function

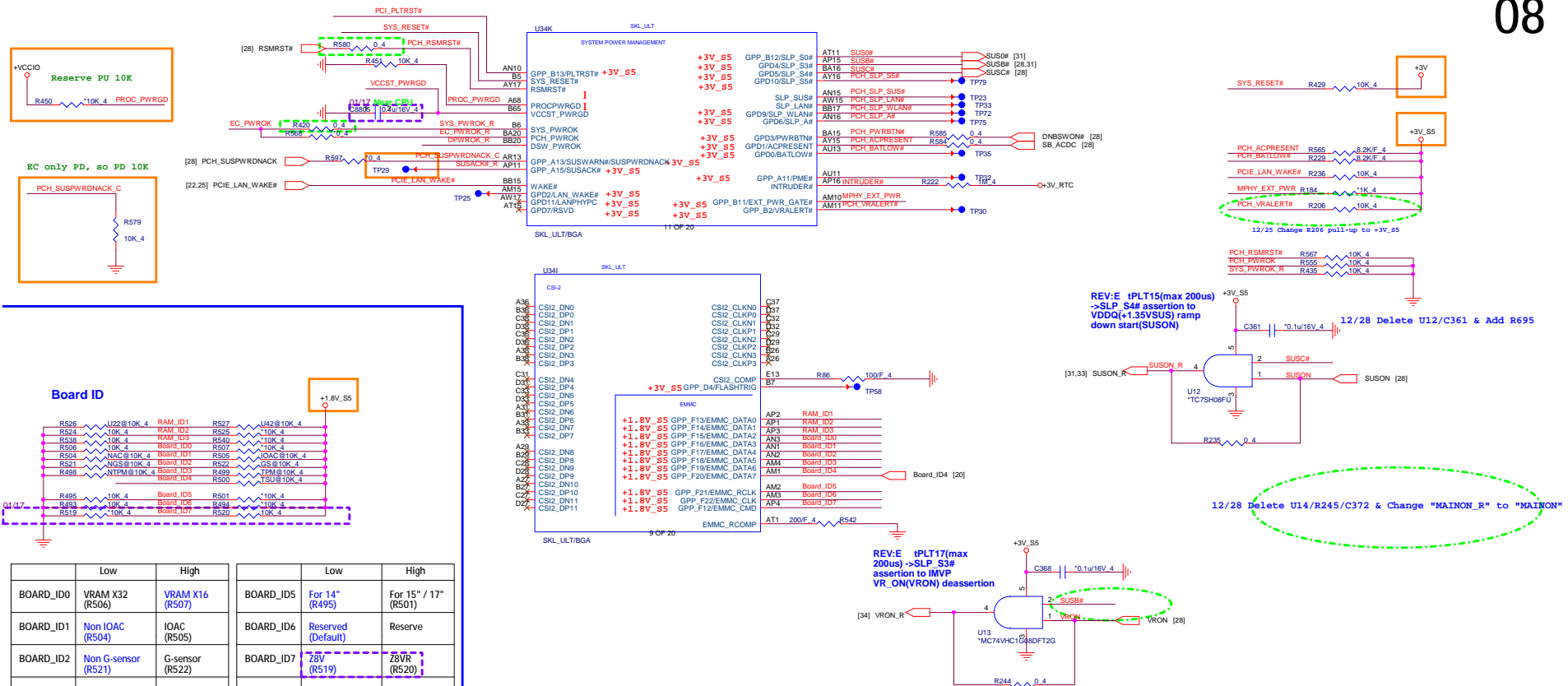


reserve for SPI fast read

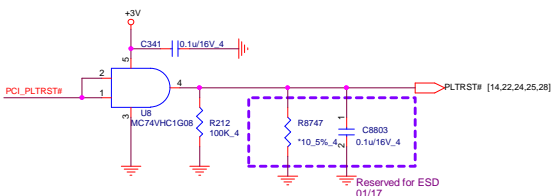


only 0ohm option

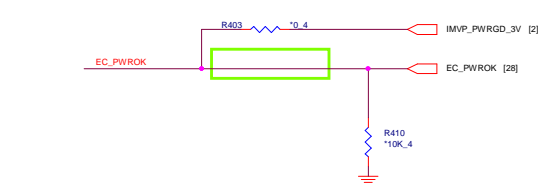




## PLTRST# Buffer



## SYSPWOK

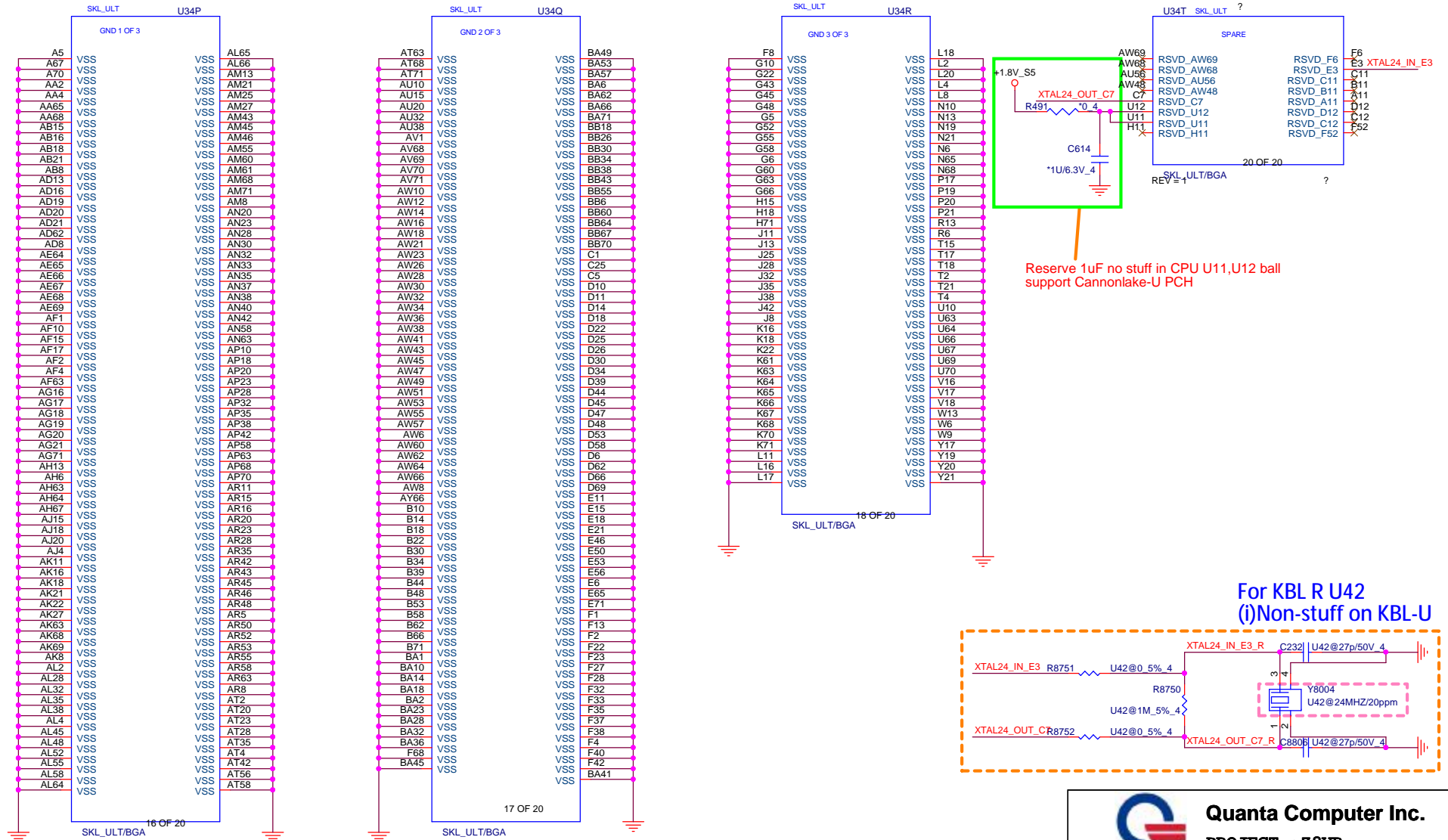




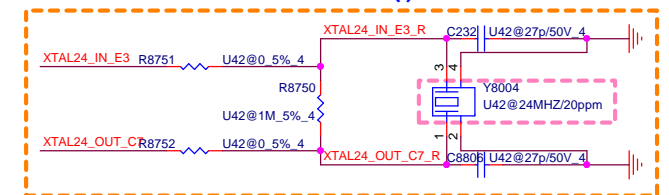


Size	Document Number	Rev
	<b>Skylake PCH-LP 15/19 (POWER)</b>	1A
Date:	Thursday, June 22, 2017	Sheet 9 of 46

## Skylake ULT (GND)



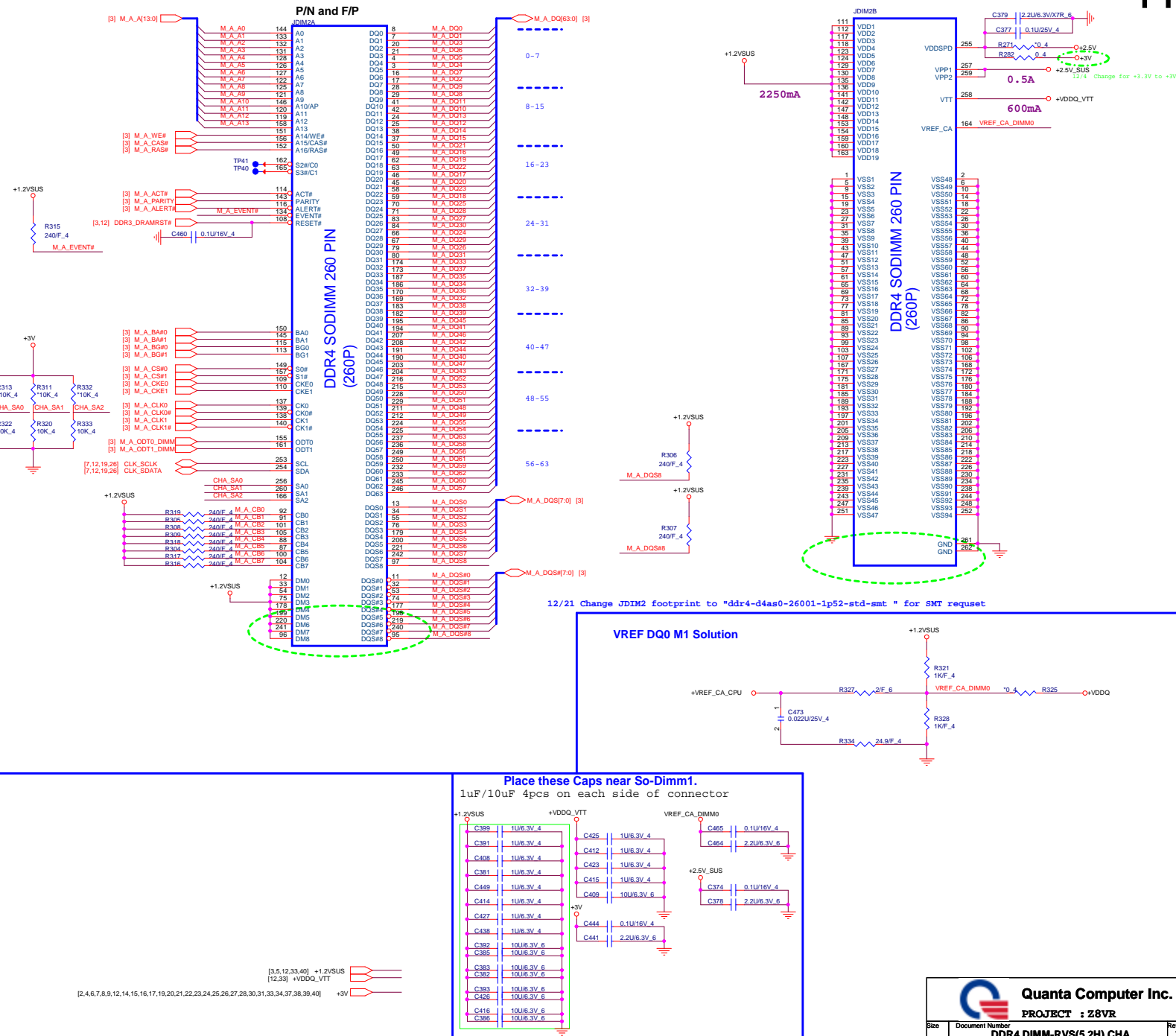
For KBL R U42  
(i)Non-stuff on KBL-U

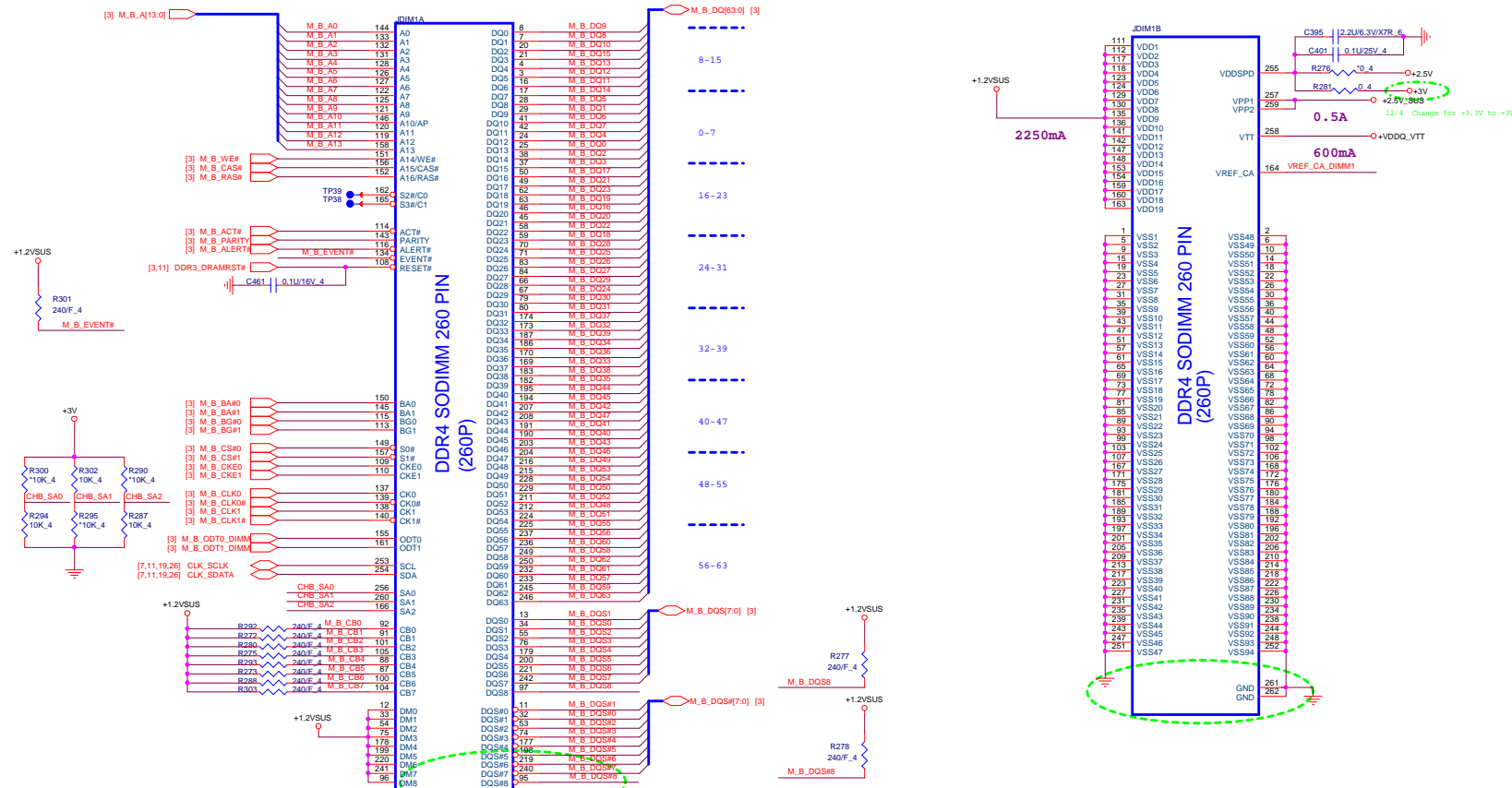
**Quanta Computer Inc.**

**PROJECT : Z8VR**

**Skylake 10/17/18 (GND)**

Size	Document Number	Rev
	<b>Skylake 10/17/18 (GND)</b>	1A
Date:	Thursday, June 22, 2017	Sheet 10 of 46



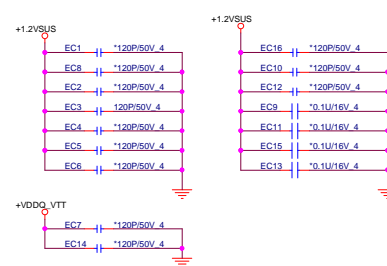


12/21 Change JDIM1 footprint to "ddr4-d4ar0-26001-1p52-rvs-smt " for SMT request

[2,4,6,7,8,9,11,14,15,16,17,19,20,21,22,23,24,25,26,27,28,30,31,33,34,37,38,39,40]

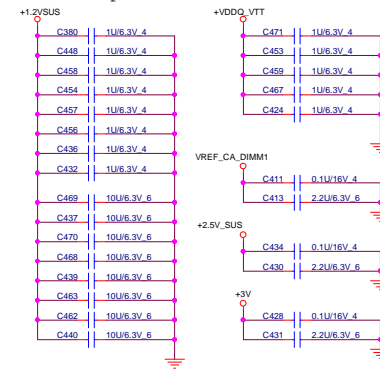
[3,5,11,33,40] +1.2VSUS

For EMI RESERVE

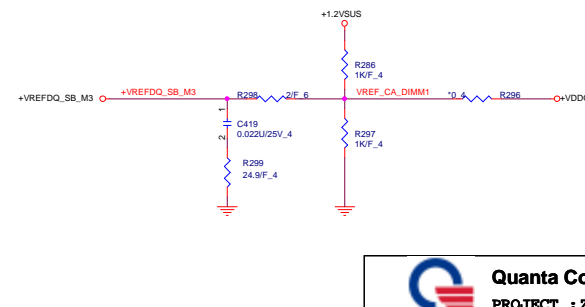


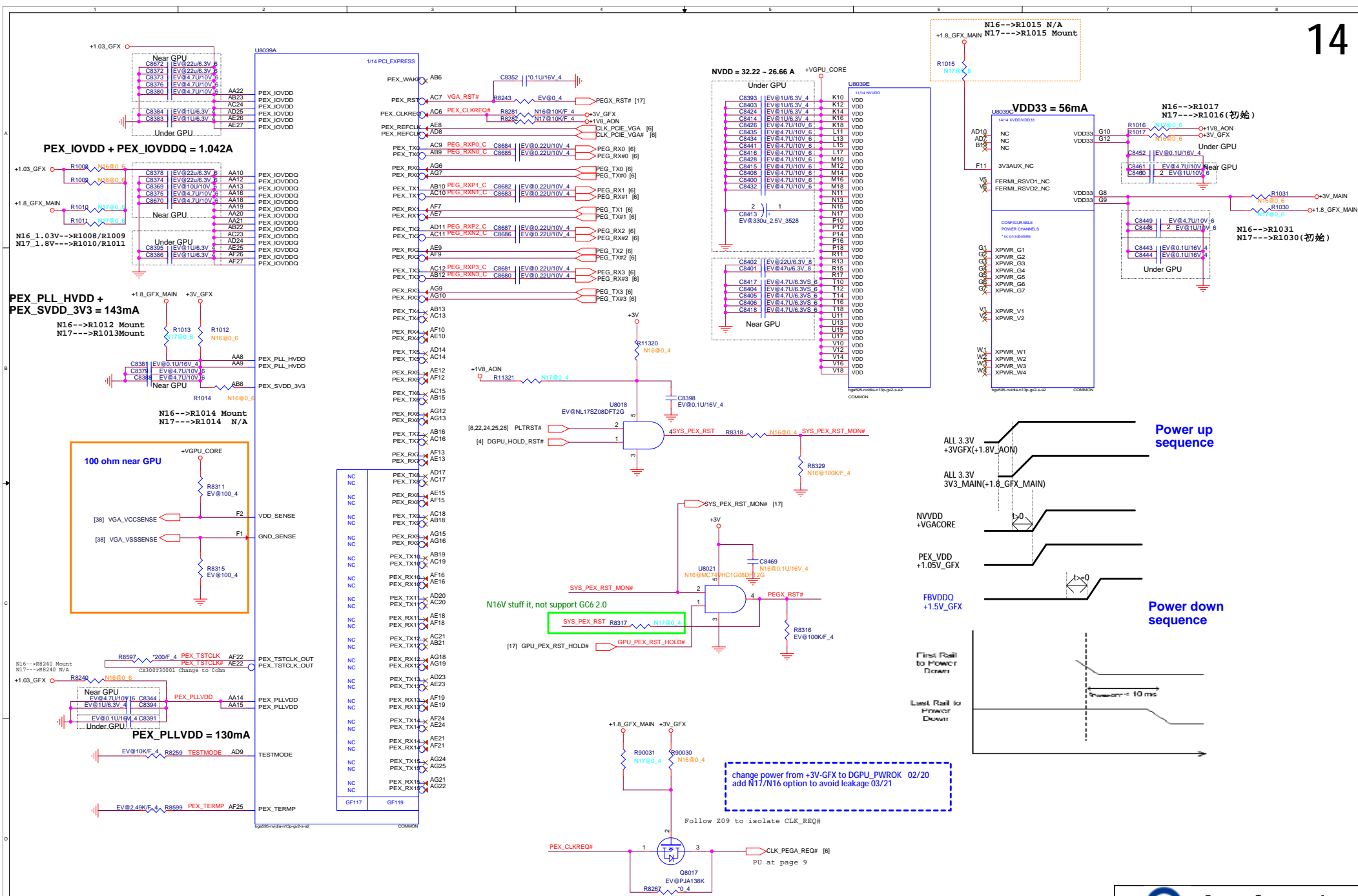
**Place these Caps near So-Dimm0.**

1uF/10uF 4pcs on each side of connector



VREF DQ1 M1 Solution

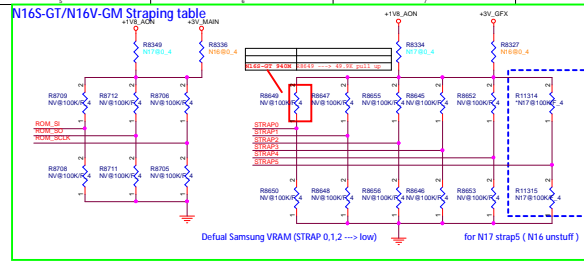












### N16S-GT DID=0x1347 [940M]

ROM\_SCLK = Stuft 4.99K pull down  
 ROM\_A0 = Stuft 4.99K pull down  
 STRAP0 = Stuft 48.9K pull up  
 STRAP1 = NC  
 STRAP2 = NC  
 STRAP3 = NC  
 STRAP4 = NC  
 ROM\_SI = VRAM Configuration follow below table

### N17S-G1-A1 DID=0x1D10 [1040]

ROM\_SI = Stuft 100K pull up  
 ROM\_A0 = Stuft 48.9K pull up  
 ROM\_SCLK = Stuft 100K pull up and Stuft 100K pull down  
 STRAP0 = VRAM Configuration follow below table  
 STRAP1 = VRAM Configuration follow below table  
 STRAP2 = Stuft 100K pull down  
 STRAP3 = Stuft 100K pull down  
 STRAP4 = Stuft 100K pull down

Note: GC6 2.0 is supported by N16x GPU in the GB28, GB48-128, and GB38-256 packages.

### Logical Strap Bit Mapping

	PU-VDD	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

### N16S-GT/N16V-GM Strapping table

ROM\_SI N16S-GT [940M]  
 2G Hynix 128Mx16 -> 34.8K PD  
 2G Micron 128Mx16 -> 45.3K PD  
 2G Samsung 128Mx16 -> 4.99K PU  
 4G Hynix 256Mx16 -> 30.1K PU Single Rank  
 4G Hynix 256Mx16 -> 24.9K PU Dual Rank  
 4G Micron 256Mx16 -> 10K PD  
 4G Samsung 256Mx16 -> 15K PD

ROM\_SO N16S-GT -> 4.99K PD  
 ROM\_SCLK N16S-GT -> 4.99K PD  
 STRAP0 N16S-GT -> 48.9K PU

N16S-GT-A2 PN : AJ0N16S0T44

N17S-G1-A1 PN : AJ0N17S0T00

### GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor (GC6 1.0)
0	OUT	GC6_FB_EN	GC6 FB Enable (GC6 2.0)
5	OUT	+3V_MAIN_EN	Enable GC6 +3V_MAIN
6	OUT	FB_CLAMP_REQ#	Active low FB Clamp toggle request (GC6 1.0)
6	IN	DGPU_EVENT#	DGPU EVENT from CPU (GC6 2.0)
8	OUT	VGA_OVTH	ACTIVE LOW THERMAL OVER TEMP
9	OUT	ALERT	ACTIVE LOW THERMAL ALERT
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding

### N16S-GT VRAM Configuration Table

### ROM\_SI

RAMCFG [3:0]	DESCRIPTION	1.35V DDR5	Vendor	Vendor PIN	ROM_SI	STN B/S
0000 0x0	DDR5 256Mx32, 64bit, 8Gb, 2500MHz		SAMSUNG B-die	K4G80325FB-HC03	PD 4.99K ohm	AKG5SGDT502
0000 0x0	DDR5 256Mx32, 64bit, 8Gb, 3000MHz		SAMSUNG B-die	K4G80325FB-HC28	PD 4.99K ohm	AKG5SGDT518
0001 0x1	DDR5 256Mx32, 64bit, 8Gb, 2500MHz		Micron A-die	MT51J256M32HF-60-A	PD 10K ohm	AKG5SGUTL04
0001 0x1	DDR5 256Mx32, 64bit, 8Gb, 3000MHz		Micron A-die	MT51J256M32HF-70-A	PD 10K ohm	AKG5SGUTL15
0101 0x5	DDR5 256Mx32, 64bit, 8Gb, 2500MHz		HYNIX M-die	H5GCH24MJR-T2C	PD 30.1K ohm	AKG5SGUTW04
0101 0x5	DDR5 256Mx32, 64bit, 8Gb, 3000MHz		HYNIX M-die	H5GCH24MJR-ROC	PD 30.1K ohm	AKG5SGUTW06

### N17S-G1-A1 VRAM Configuration Table

### STRAP0, STRAP1, STRAP2

RAMCFG [3:0]	DESCRIPTION	1.35V DDR5	Vendor	Vendor PIN	STRAP0	STRAP1	STRAP2	STN B/S
0000 0x0	DDR5 256Mx32, 64bit, 8Gb, 3000MHz		SAMSUNG B-die	K4G80325FB-HC28	PD 100K ohm	PD 100K ohm	PD 100K ohm	AKG5SGDT518
0001 0x1	DDR5 256Mx32, 64bit, 8Gb, 3000MHz		Micron A-die	MT51J256M32HF-70-A	PU 100K ohm	PD 100K ohm	PD 100K ohm	AKG5SGUTL15
0010 0x2	DDR5 256Mx32, 64bit, 8Gb, 3000MHz		HYNIX M-die	H5GCH24MJR-ROC	PD 100K ohm	PU 100K ohm	PD 100K ohm	AKG5SGUTW06

Non-mirror, MF=0 Channel A  
<0-31>

Mirror, MF=1

Channel A  
<32-63>

DQA24~31

DQA16~23

DQA8~15

DQA0~7

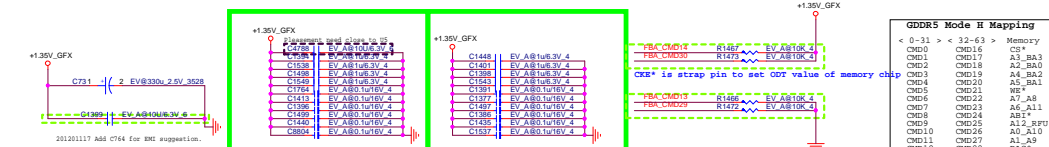
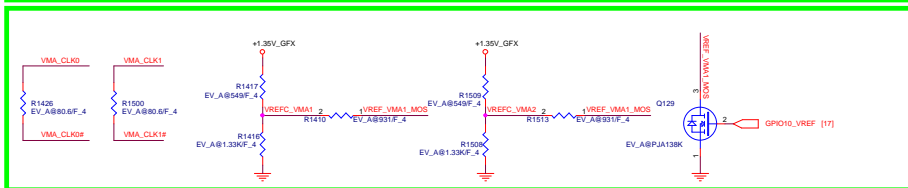
DQA32~39

DQA40~47

DQA48~55

DQA56~63

KB OnlyA



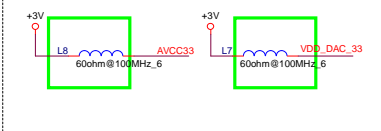
GDDR5 Mode H Mapping

< 0-31 >	< 32-63 >	Memory
CHD0	CHD16	CS*
CHD1	CHD17	A1_BA3
CHD2	CHD18	A2_BA0
CHD3	CHD19	A1_BA2
CHD4	CHD20	A2_BA1
CHD5	CHD21	RE*
CHD6	CHD22	A7_A8
CHD7	CHD23	A6_A11
CHD8	CHD24	ABT*
CHD9	CHD25	A12_RP0
CHD10	CHD26	A1_A10
CHD11	CHD27	A1_A9
CHD12	CHD28	RA0*
CHD13	CHD29	RS0*
CHD14	CHD30	CS0*
CHD15	CHD31	CA0*

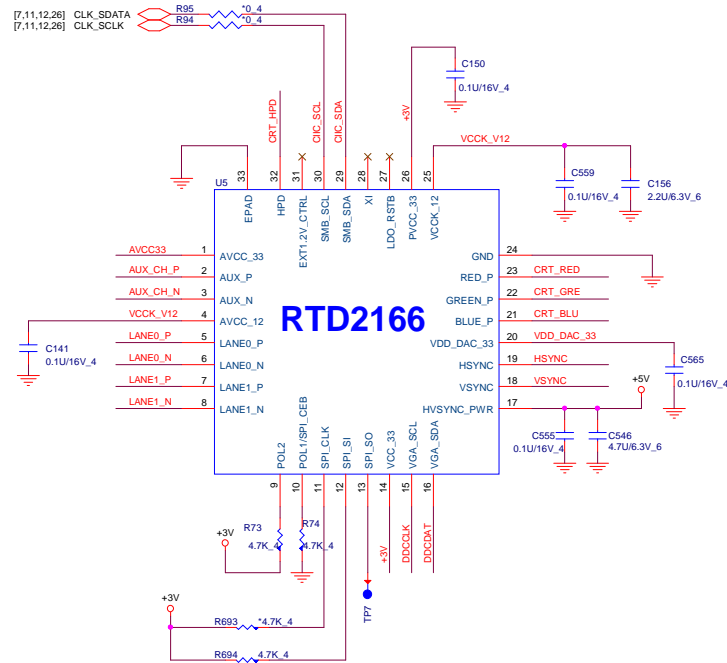
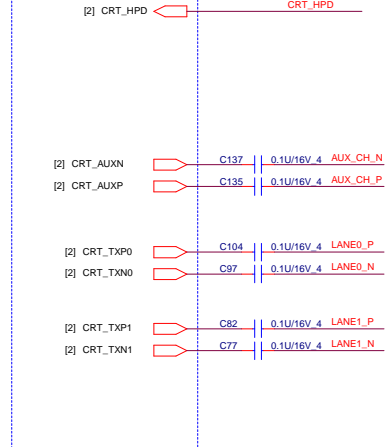
RST PD place @ the end of daisy-chain.

## DP TO VGA

## Power



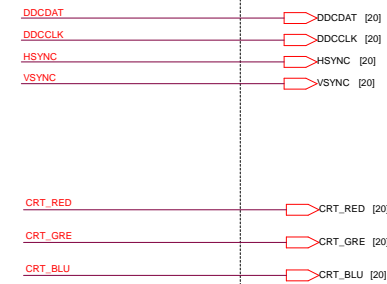
## CPU



## Note:

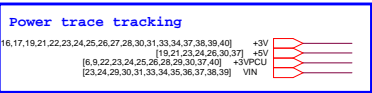
- 1- C1,C3,C4,C5,C11,C16, C21 should be placed close to chip
- 2- C5 should be X5R material
- 3- R6, R7, R8 should be 75 ohm with +/-1%
- 4- Suggest to connect Pin 29 and Pin 30 to PCH SMBUS for debug purpose.
- 5- This configuration is for internal ROM mode and using embedded LDO mode.

## VGA

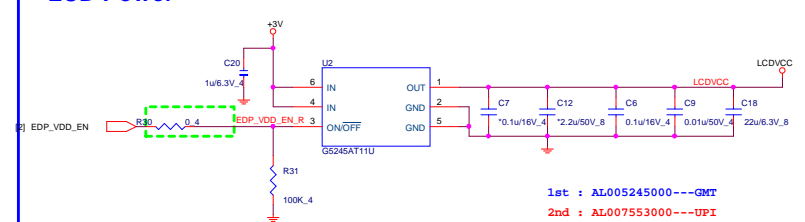


[2,4,6,7,8,9,11,12,14,15,16,17,20,21,22,23,24,25,26,27,28,30,31,33,34,37,38,39,40] +3V  
[20,21,23,24,26,30,37] +5V

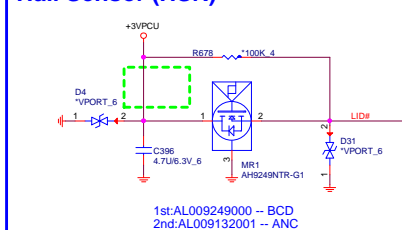
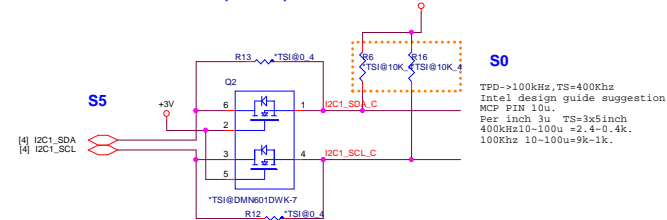
## 20



## LCD Power



1st : AL005245000---GMT  
2nd : AL007553000---UPI



## HDMI

&lt;HDM&gt;

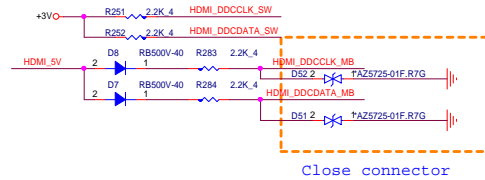
OE_N	DDC_EN	HPD_SINK	Source output	PTN3366 power mode
LOW	HIGH	HIGH	source active	Active mode: DDC active
LOW	LOW	LOW	don't care	Standby mode
HIGH	LOW	don't care	don't care	Ultra low-power mode

From PCH

## HDMI-detect

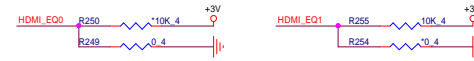
S5 input high

S0



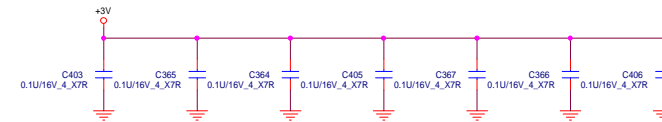
Power trace tracking

[2,4,6,7,8,9,11,12,14,15,16,17,19,20,22,23,24,25,26,27,28,30,31,33,34,37,38,39,40]  
[19,20,23,24,26,30,37]

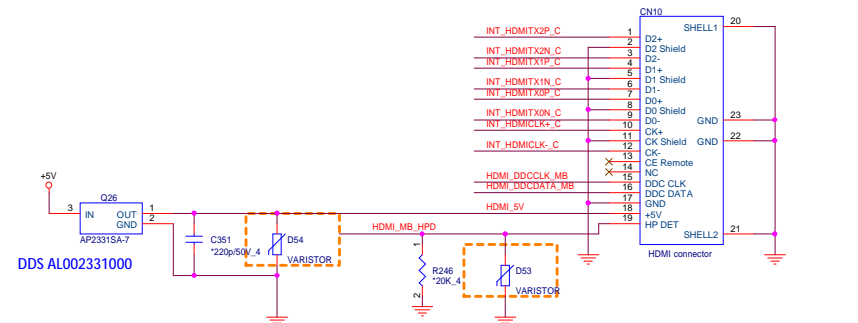
+3V  
+5V

Inputs	EQ0	Equalization for 3 Gbit/s
EQ1 short to GND	short to GND	0 dB
short to GND	short to Vcc	2 dB
short to VDD	short to GND	4 dB
short to VDD	short to Vcc	6 dB

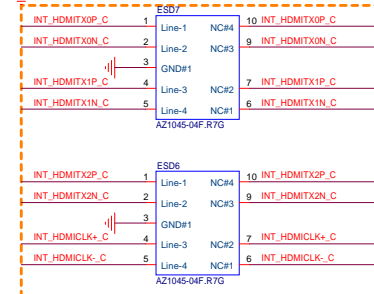
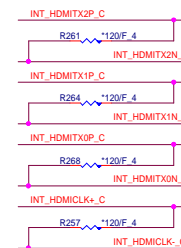
21



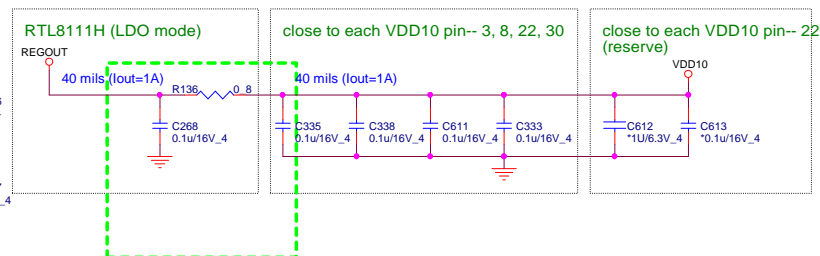
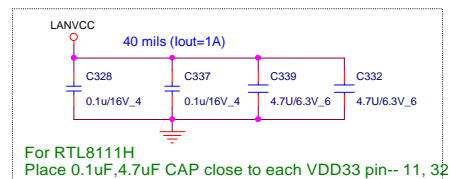
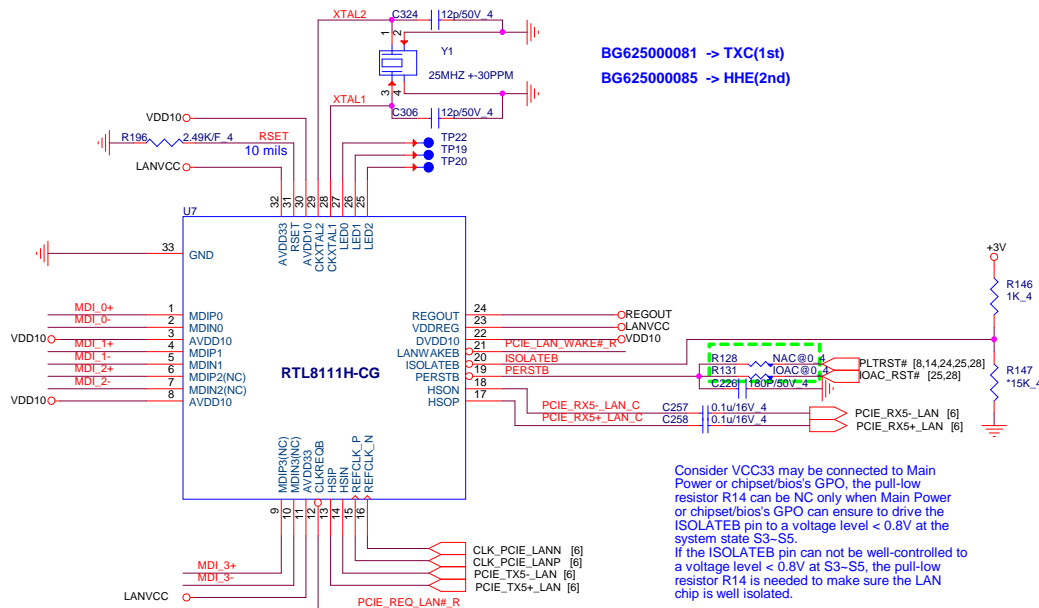
## HDMI connector



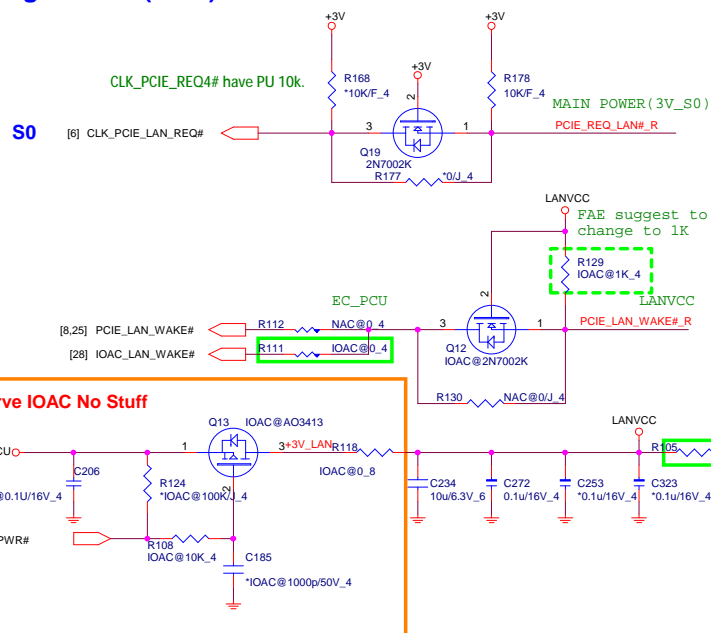
## EMI



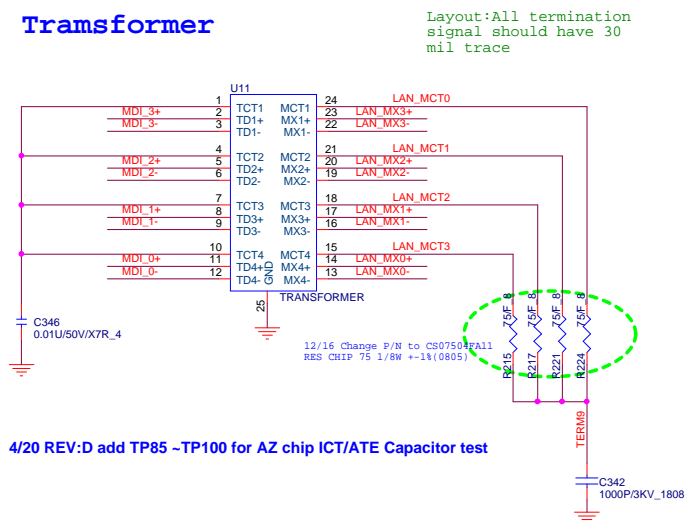




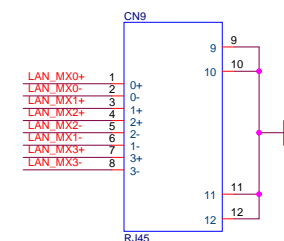
## Leakage circuit (MPC)



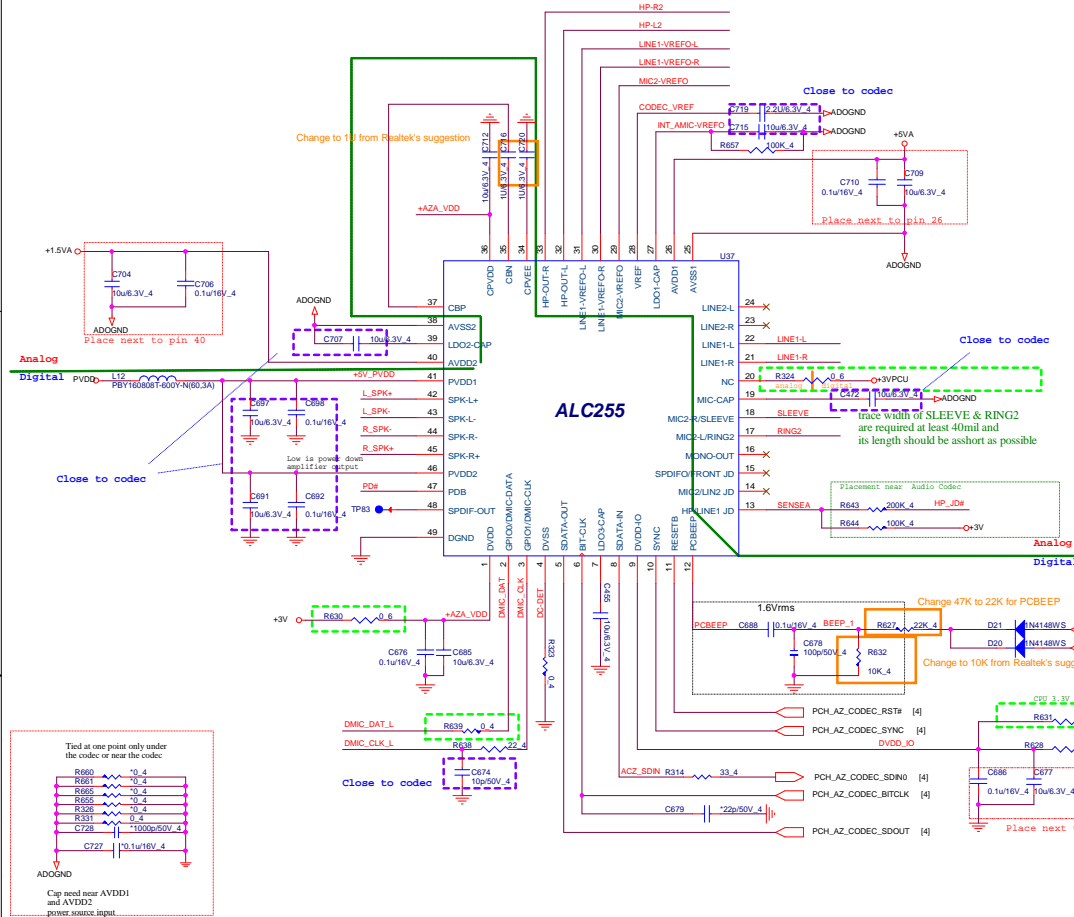
## Transformer



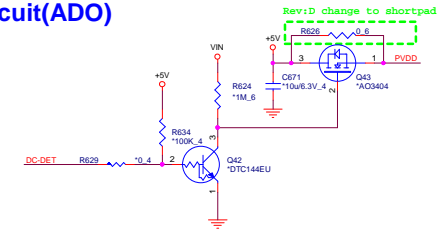
## RJ45 Connector



## Codec(ADO)

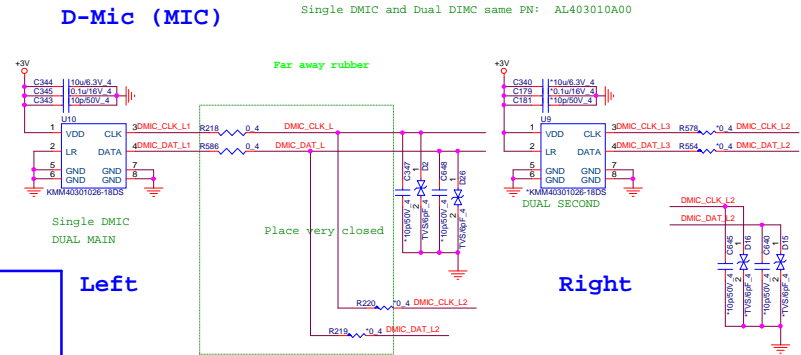


## DC-DET circuit(ADO)

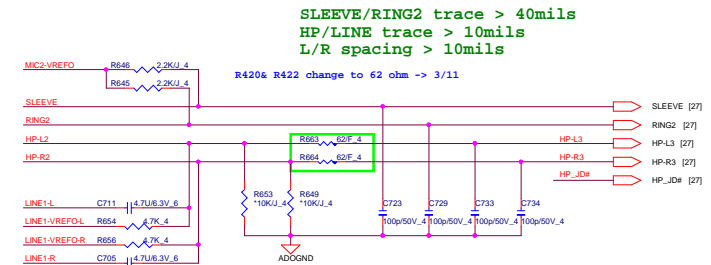


23

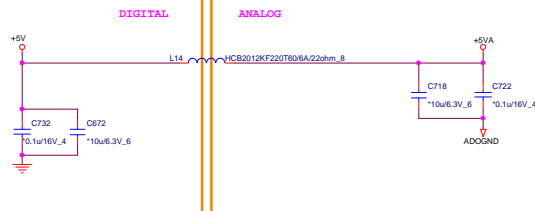
## D-Mic (MIC)



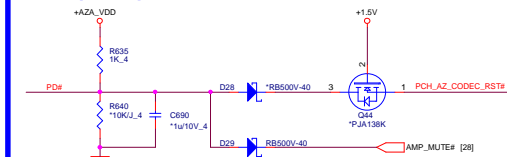
## Universal Audio Jack HEADPHONE/MIC/LINE combo (ADO)



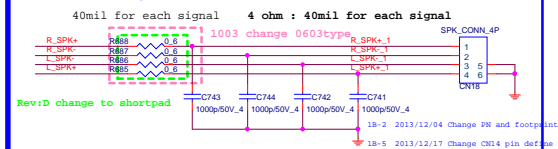
## Codec PWR 5V(ADO)



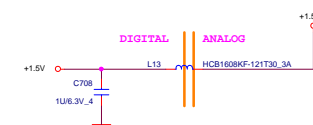
## Mute(ADO)



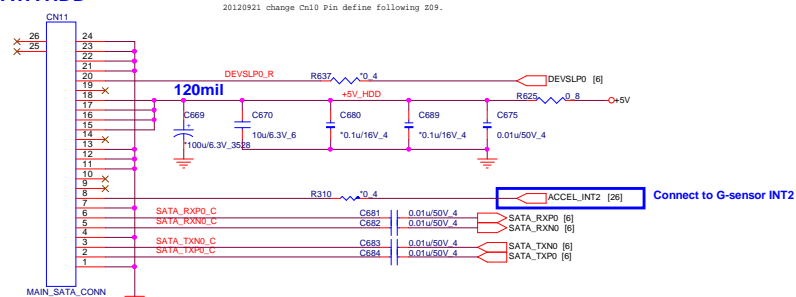
## Internal Speaker



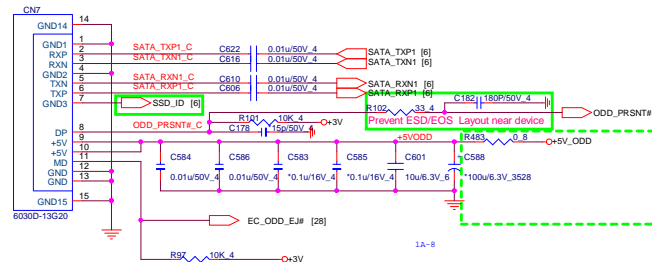
## Codec PWR 1.5V(ADO)



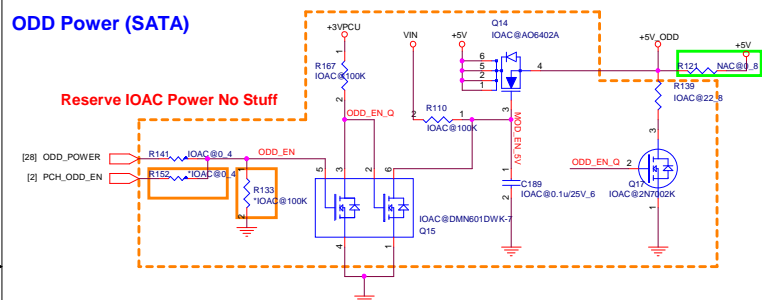
**SATA HDD**



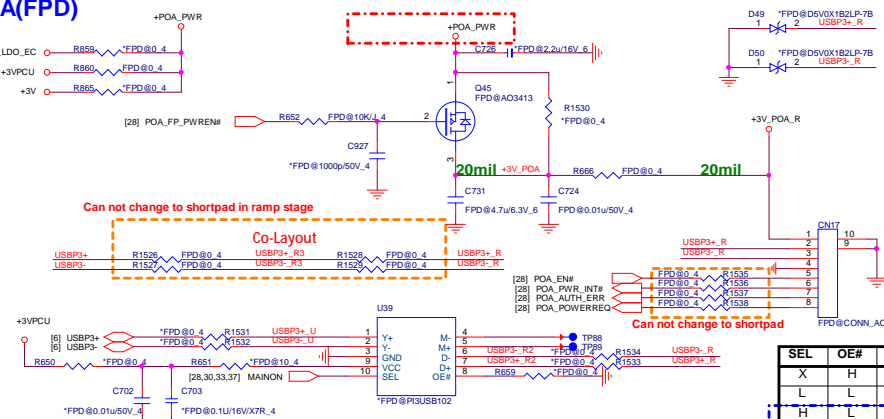
### SATA ODD Connector



ODD Power (SATA)



**POA(FPD)**



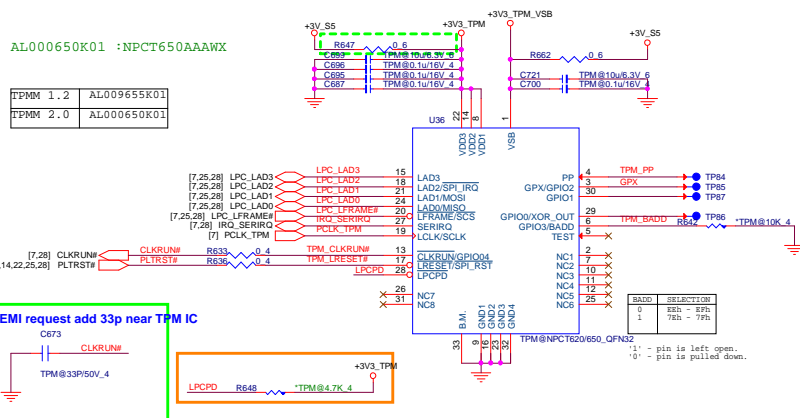
SEL	OE#	Y+	Y-
X	H	Hi-Z	Hi-Z
L	L	M+	M-
H	L	D+	D-

Spec define: High Active

### TPM NPCT650 (TPM)

SP@ BOM周邊上NPCT650  
A,B,C P/N:AL009655K01(SLB9655TT1.2- FW4.31)  
RAMP P/N: AL000650K01 (NPCT650AAAWX)

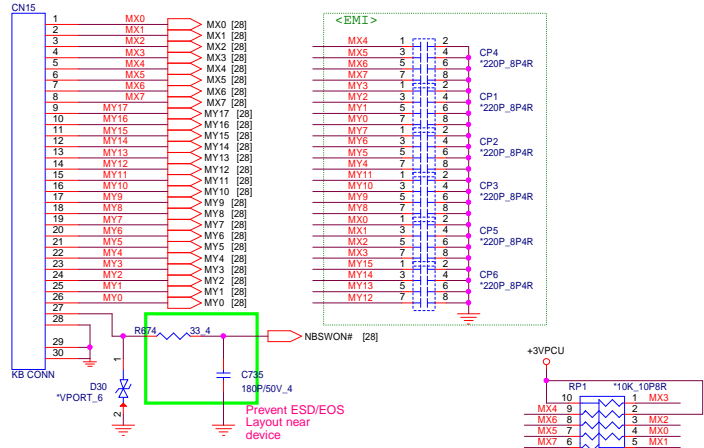
AL000650K01 :NPCT650AAAWX



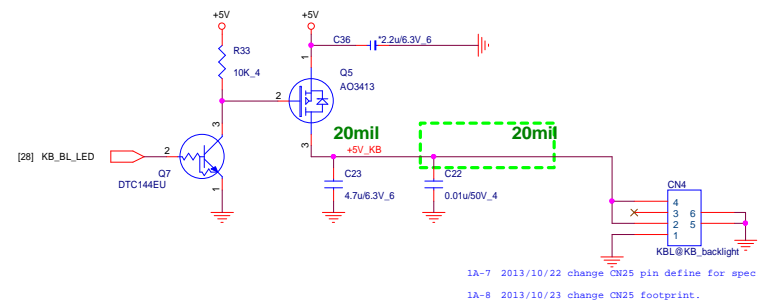
12/30 Modify Hole1、Hole14、Hole17 to NC



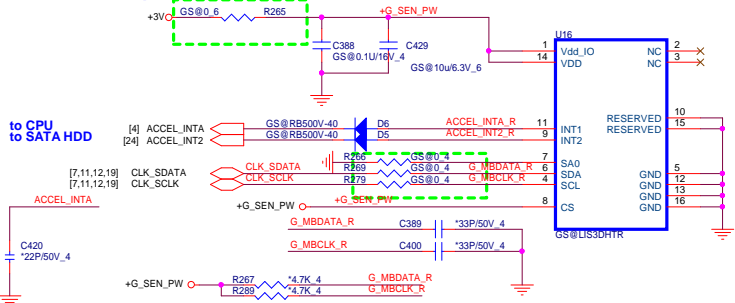
## KEYBOARD (KBC)



## KB\_BL LED (KBC)

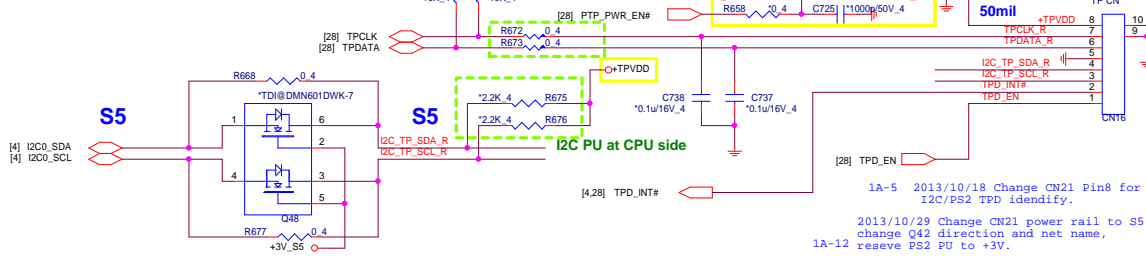


## G-sensor(ACS)



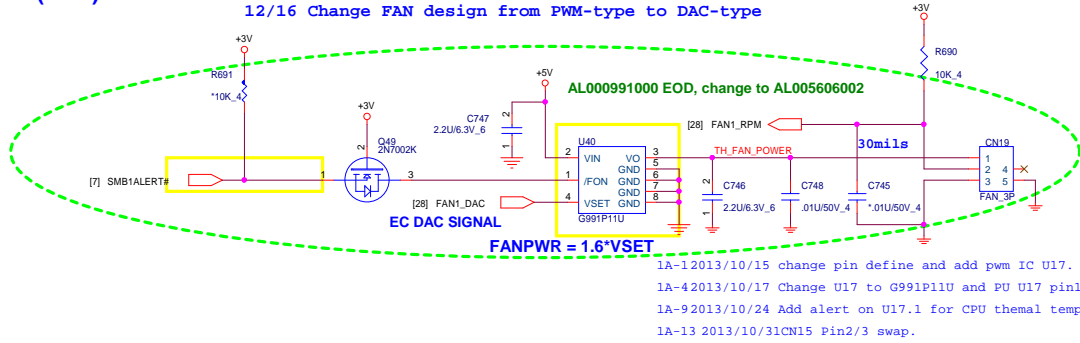
## TOUCHPAD BOARD CONN (TPD I2C/PS2 co-lay)

TPD->100kHz, TS=400kHz  
Intel design guide suggestion  
MCP PIN 10u.  
Per inch 3u TS=3x5inch  
400kHz±10-100u=2.4-0.4k.  
100kHz 10-100u=9k-1k.



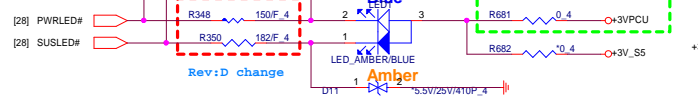
## CPU FAN (THM)

12/16 Change FAN design from PWM-type to DAC-type

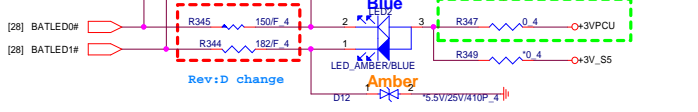


## POWER LED(UIF)

### Power LED

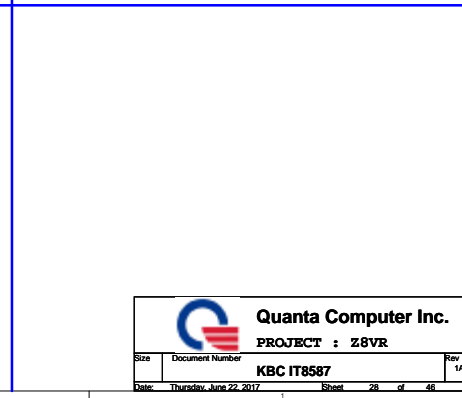
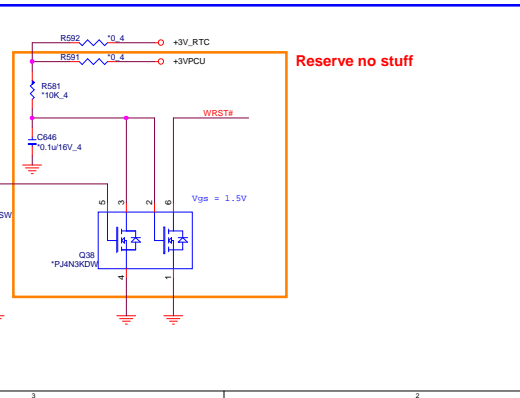
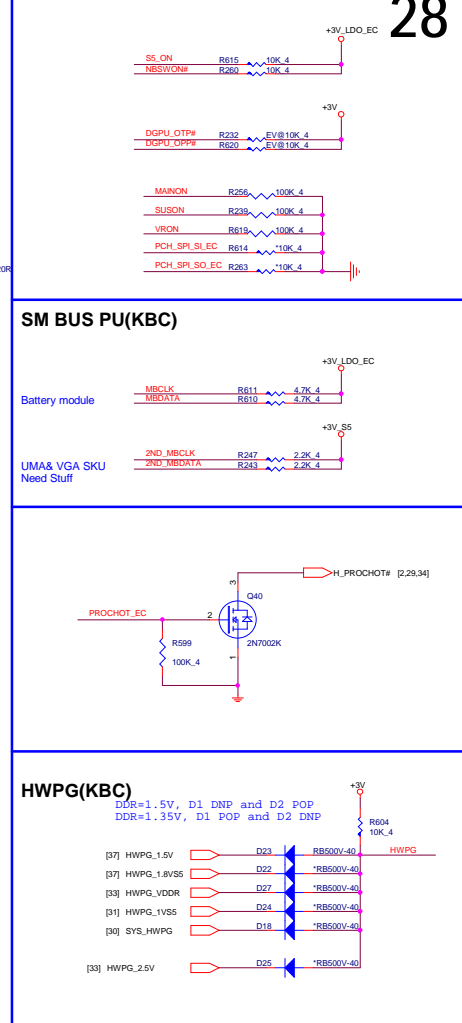


### Battery



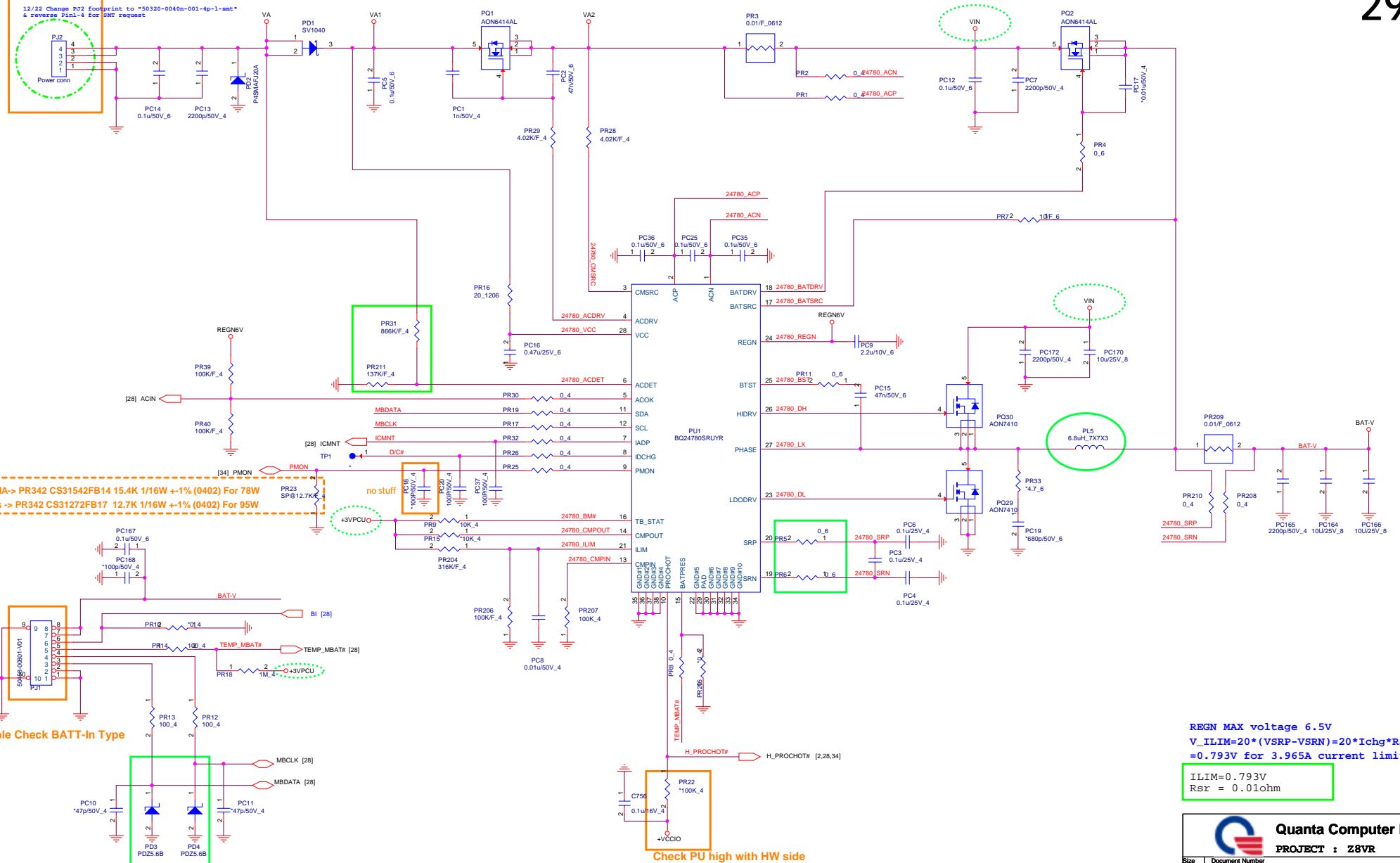




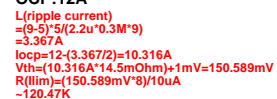


## Double Check ADP-In Type

12/22 Change P02 footprint to \*03320-0040n-001-4p-1-mnt\* & reverse Pin1-4 for HW request

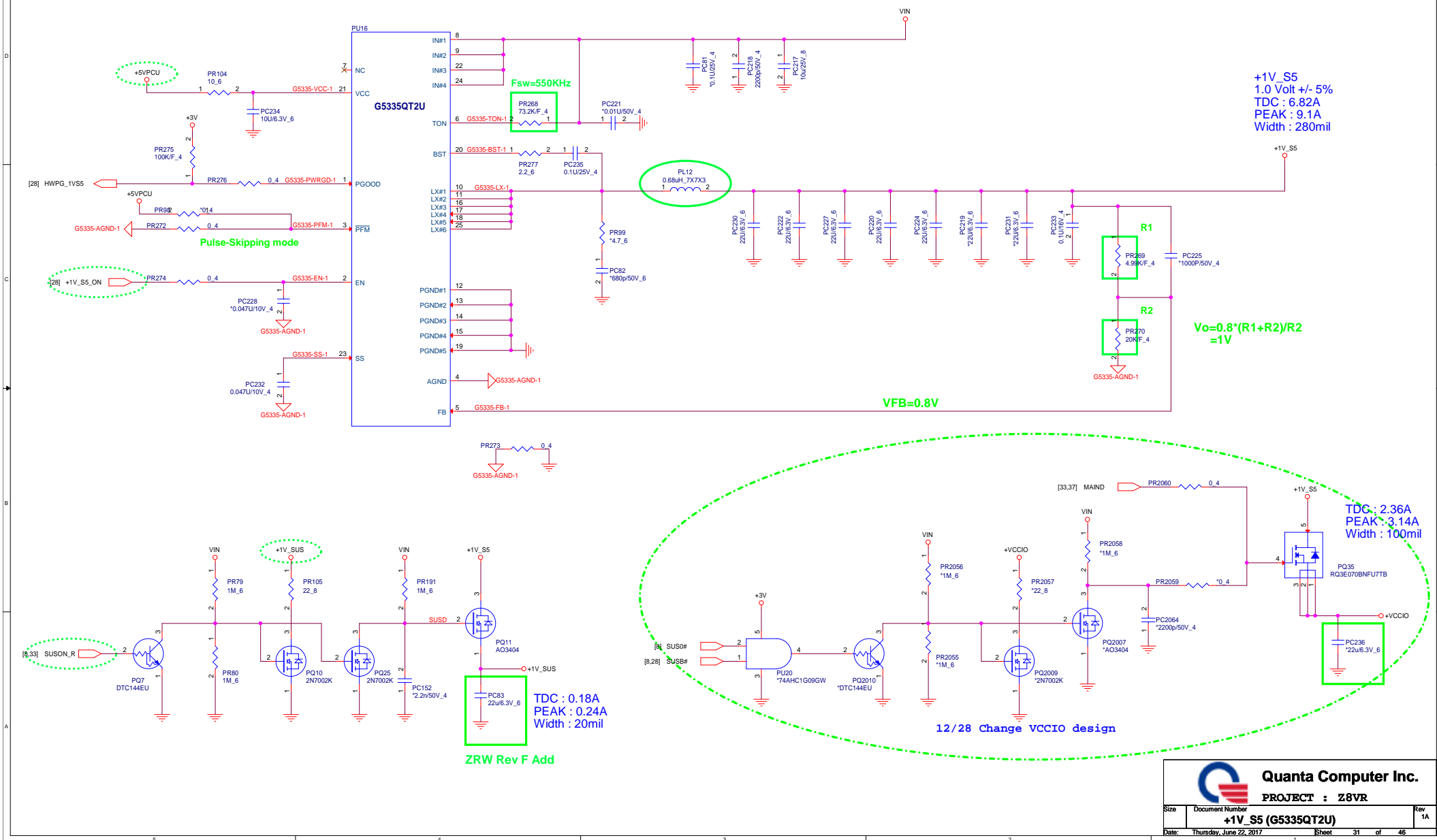


REGN MAX voltage 6.5V  
 $V_{ILIM} = 20 \times (V_{SRP} - V_{SRN}) = 20 \times I_{chg} \times R_{sr} = 0.793V$  for 3.965A current limit  
 $ILIM = 0.793V$   
 $R_{sr} = 0.01\Omega$

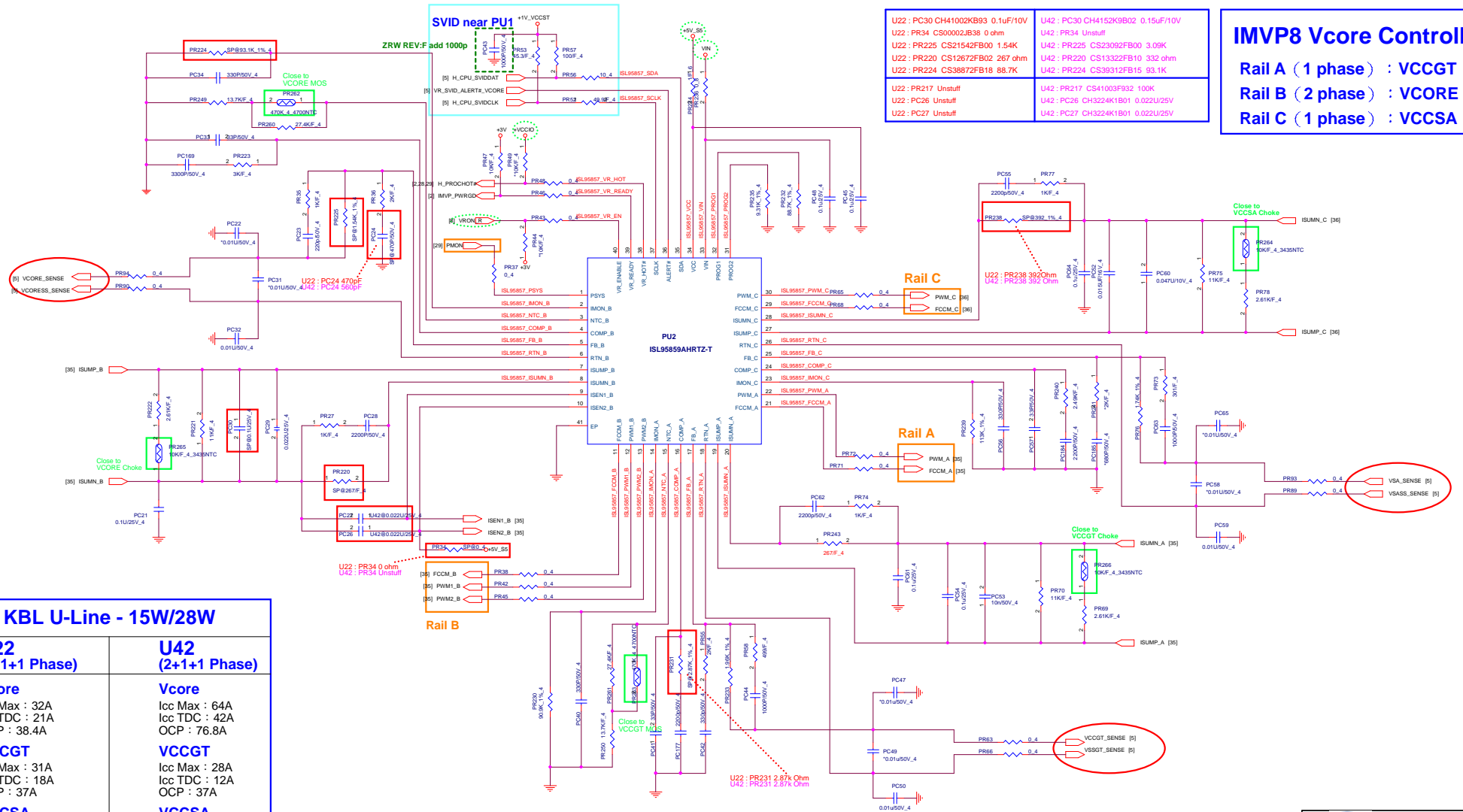


$L(\text{ripple current}) = (9-3.3) \cdot 3.3 / (2.2 \mu \cdot 0.355 \text{M} \cdot 9) = 2.676 \text{A}$   
 $I_{\text{ocp}} = 10 - (2.676/2) = 8.662 \text{A}$   
 $V_{\text{th}} = (8.662 \text{A} \cdot 14.5 \text{m}\Omega) + 1 \text{mV} = 126.599 \text{mV}$   
 $R(\text{Ilim}) = (126.599 \text{mV}^2 / 8) / 10 \mu \text{A} = 101.279 \text{k}\Omega$









KBL U-Line - 15W/28W	
U22 (1+1+1 Phase)	U42 (2+1+1 Phase)
<b>Vcore</b> Icc Max : 32A Icc TDC : 21A OCP : 38.4A  <b>VCCGT</b> Icc Max : 31A Icc TDC : 18A OCP : 37A  <b>VCCSA</b> Icc Max : 4.5A OCP : 10A	<b>Vcore</b> Icc Max : 64A Icc TDC : 42A OCP : 76.8A  <b>VCCGT</b> Icc Max : 28A Icc TDC : 12A OCP : 37A  <b>VCCSA</b> Icc Max : 5A OCP : 10A

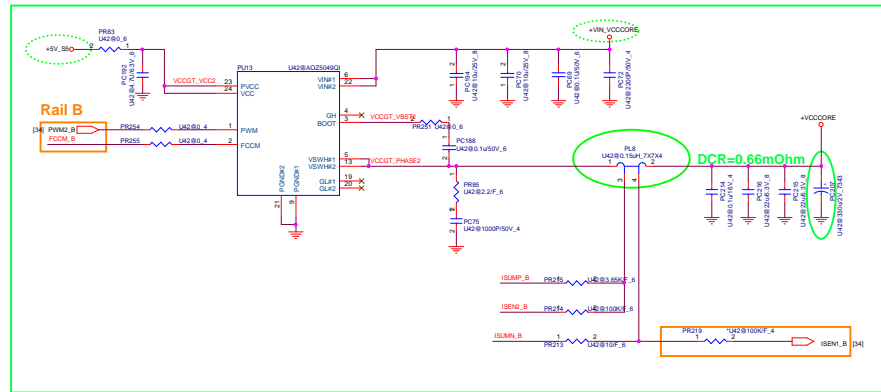
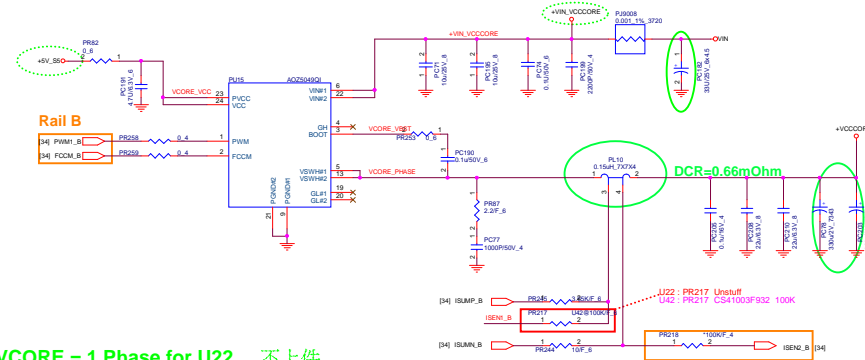


[26,23,24,29,30,31,33,34,36,37,38,39] VIN  
 [8] +VCCORE  
 [9] +VCCGT  
 [27,30,33,34,36,38,39,40] +5V, 5S

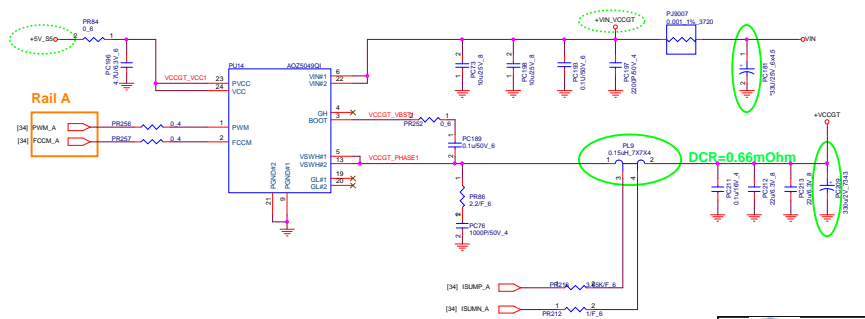
U22: PR217 Unstuff

U42: PR217 CS41003F932 100K

## VCORE



## VCCGT



**VCCSA**

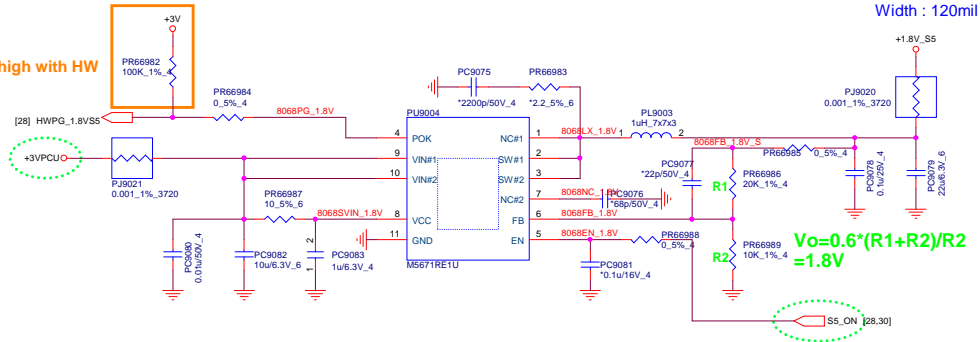
R_AC_LL : 10.3mV/A
--------------------



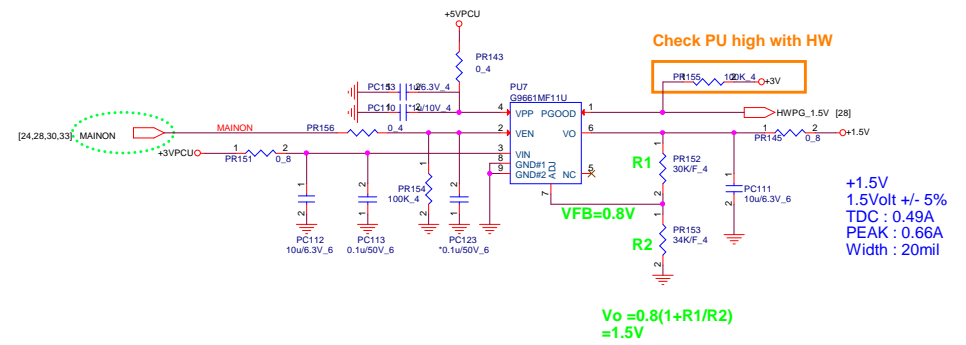
**PROJECT : Z8VR**

Size	Document Number	Rev
	<b>VCCSA (ISL95808HRZ-T)</b>	1A
Date:	Thursday, June 22, 2017	Sheet 36 of 46

Check PU high with HW

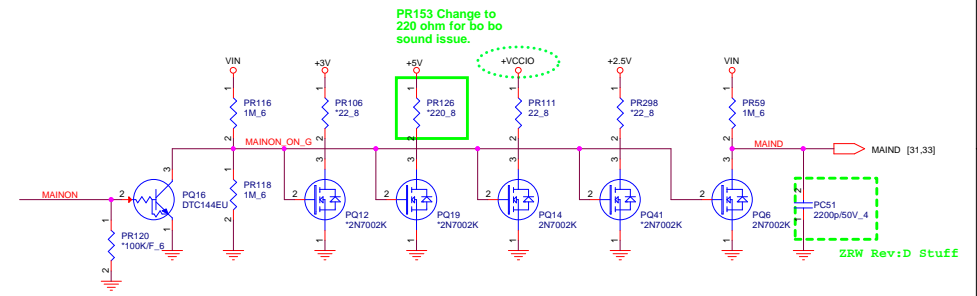
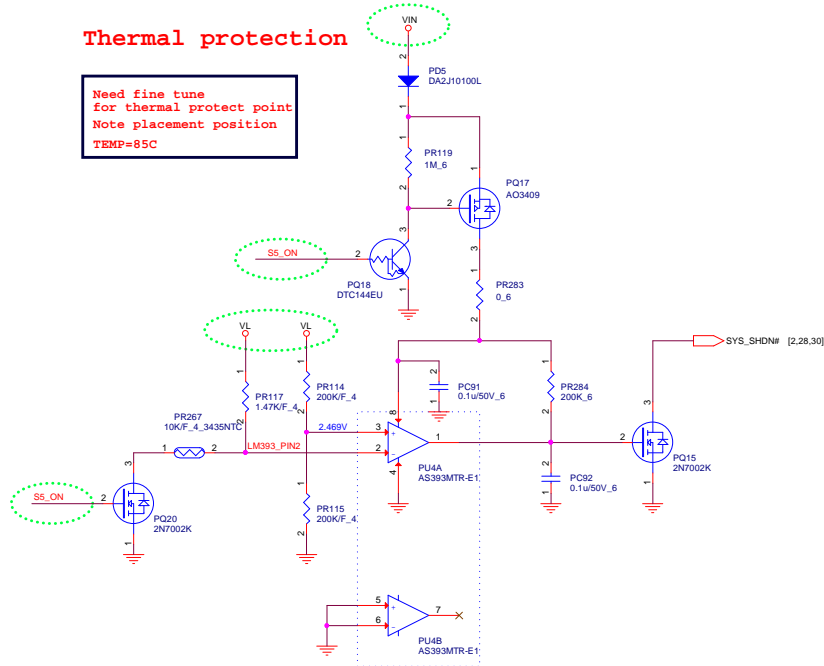


Check PU high with HW



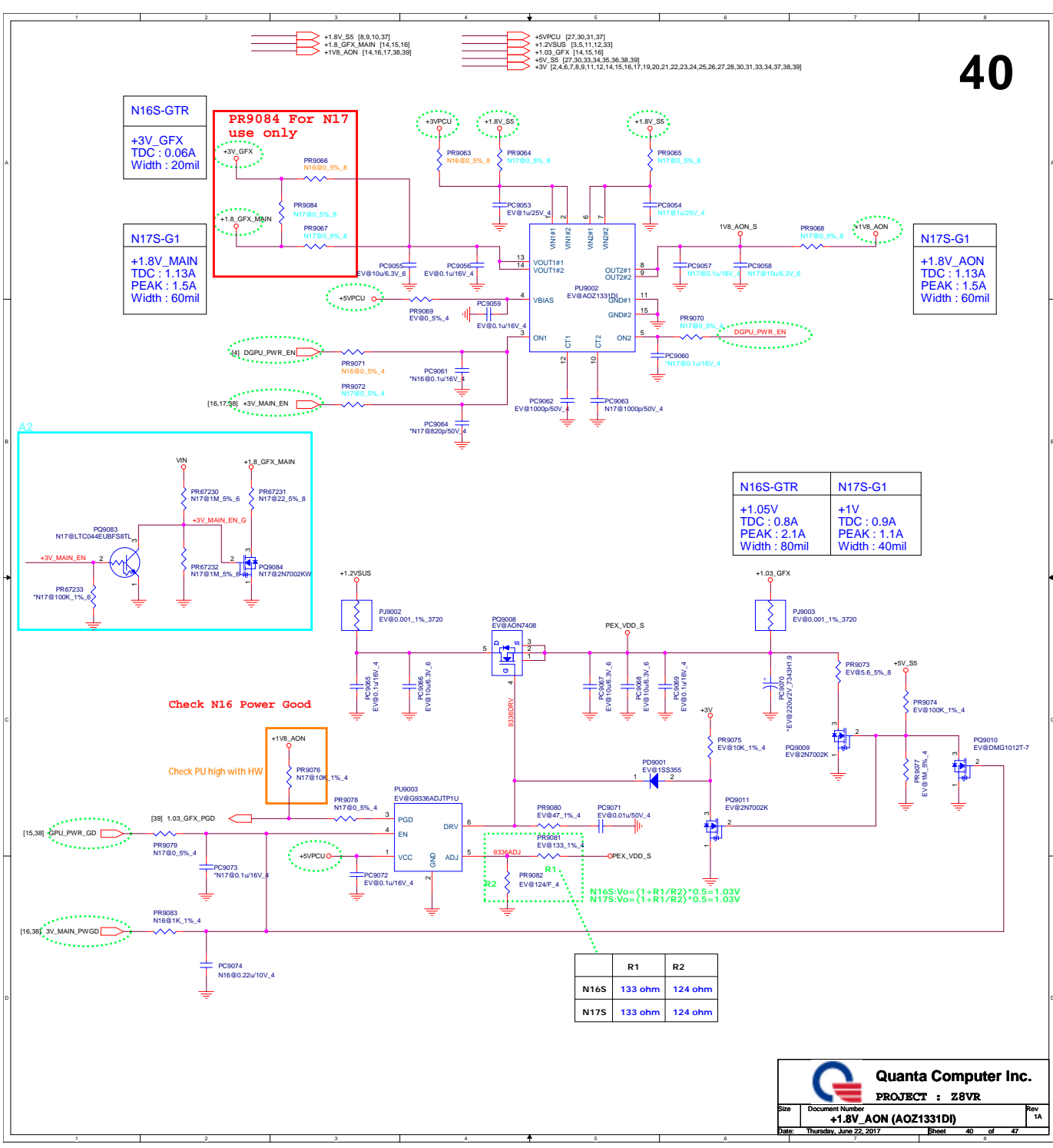
## Thermal protection

Need fine tune  
for thermal protect point  
Note placement position  
TEMP=85C









N16S-GTR	N17S-G1
+1.05V TDC : 0.8A PEAK : 2.1A Width : 80mil	+1V TDC : 0.9A PEAK : 1.1A Width : 40mil

Check N16 Power Good

Check PU high with HW

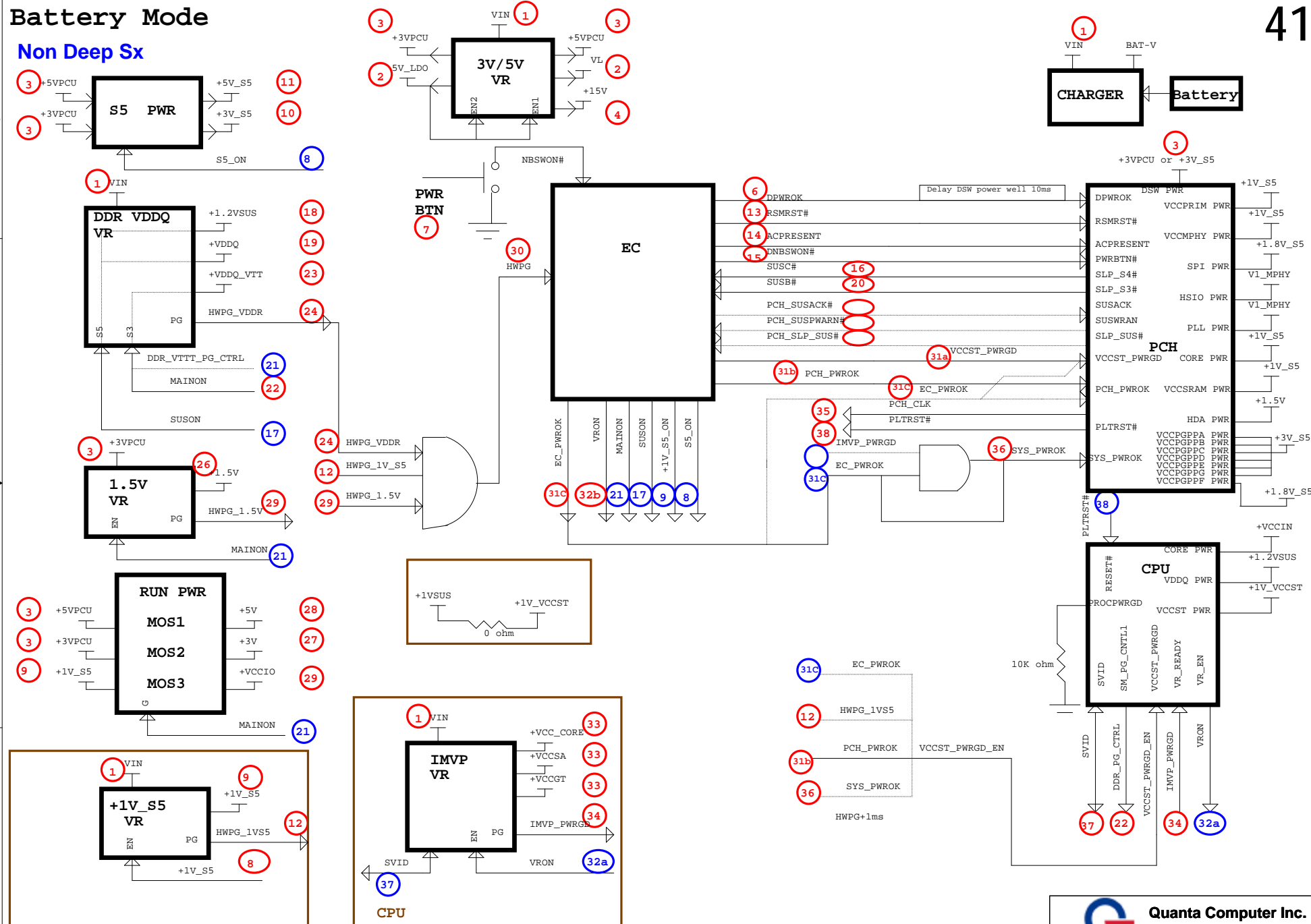
$$\begin{aligned} \therefore N16S:V_o &= (1 + R1/R2) * 0.5 = 1.03V \\ \therefore N17S:V_o &= (1 + R1/R2) * 0.5 = 1.03V \end{aligned}$$

	R1	R2
N16S	133 ohm	124 ohm
N17S	133 ohm	124 ohm

# Battery Mode

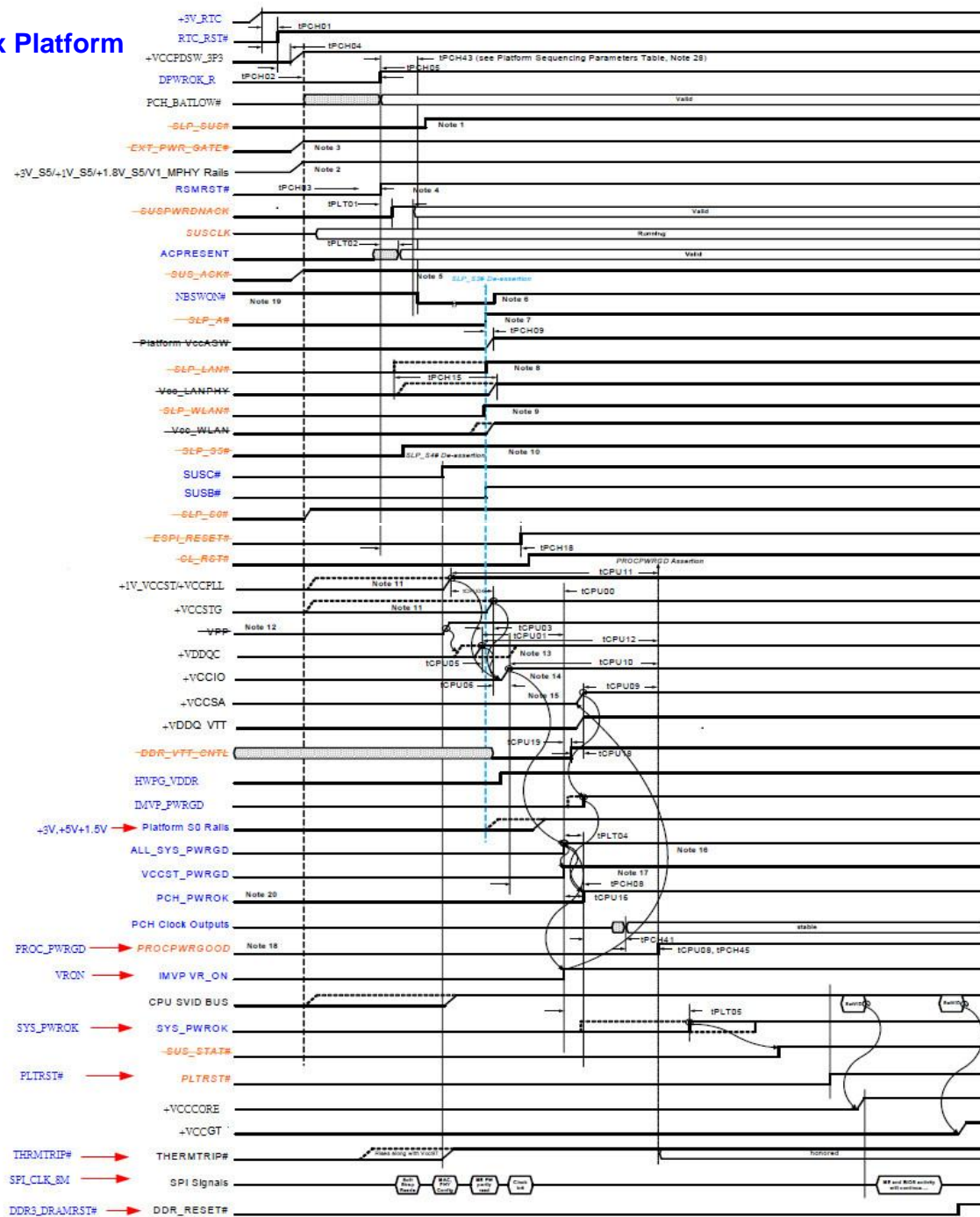
## Non Deep Sx

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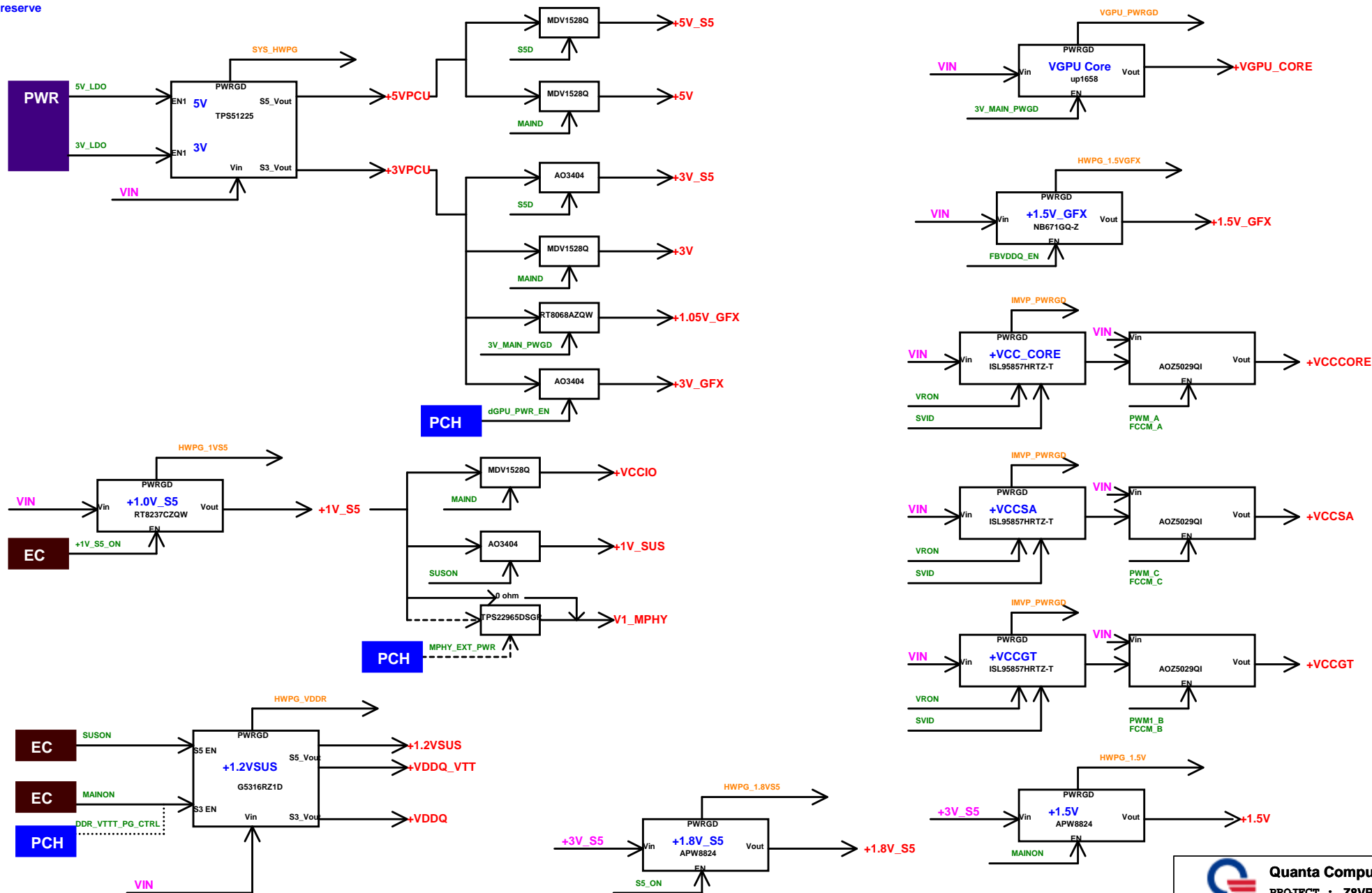


# Skylake U Non-Deep Sx Platform Power on sequence

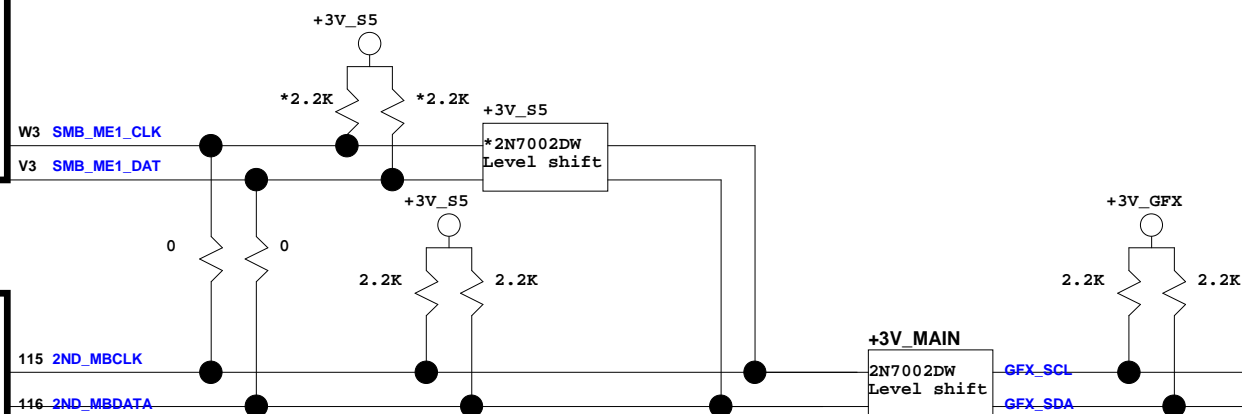
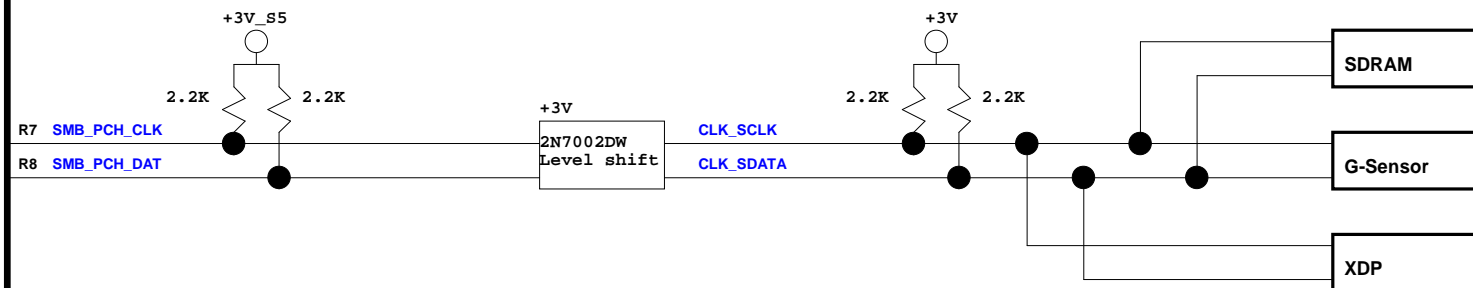


實線表default  
虛線表reserve

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Skylake U

EC  
IT8987CX